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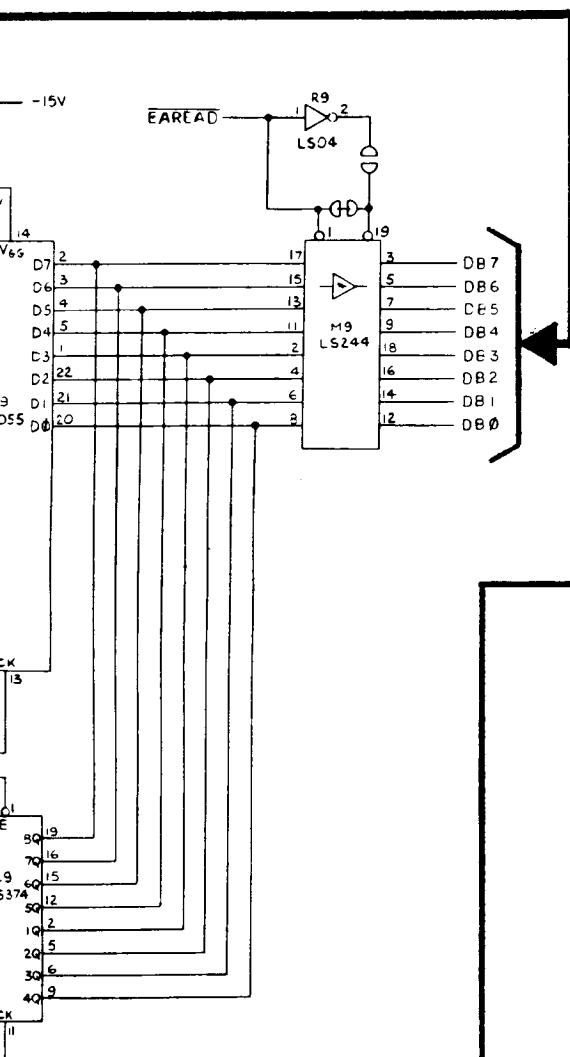


FLIPPERSPILL.COM

1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

R
R
R
R

Program ROM
Program ROM
Program ROM
Program ROM



The High Score Memory circuit consists of an erasable re-programmable ROM N9, latches L9, P9, N10 buffer M9, and timer N11.

N11 produces a 12KHz 0-15V squarewave. This signal when + 15, forward biases diode CR4 and allows capacitor C50 to charge th -29V. When it's OV, CR4 is then cut-off and CR3 is forward biased which causes C49 to develop a charge. C49 charges to approximately -28V. This is the potential required for EAROM N9 to operate.

The MPU addresses the EAROM (AB0-AB5) via latch N10, when EAADDR1 goes high, and data is latched into the EAROM on DB0-DB7 through latch L9.

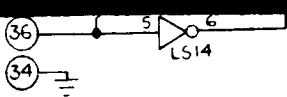
The function of the EAROM (read, write or erase) is determined by the MPU on data lines DB0-DB3. Latch D9 receives a high EACONTROL signal from the MPU address decoder and function data is passed to the EAROM.

Data in the EAROM is read by the MPU when the EAREAD is addressed by the MPU after a reset pulse or during self-test.

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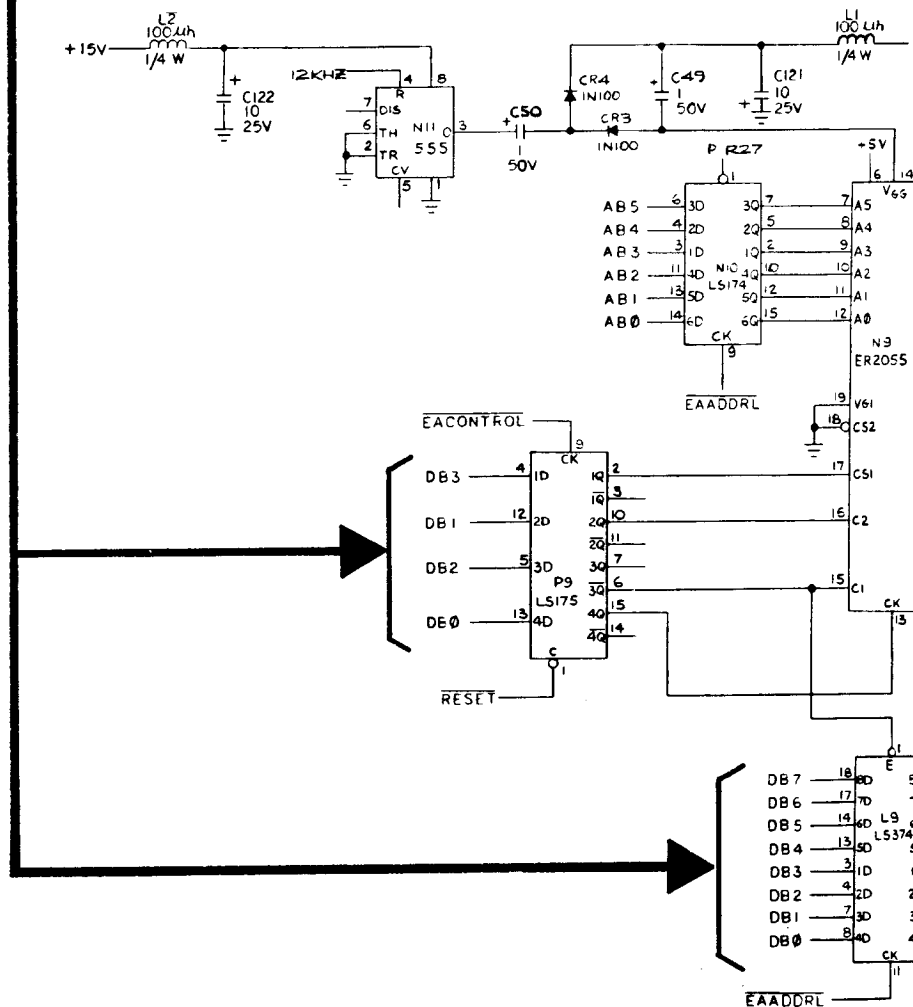
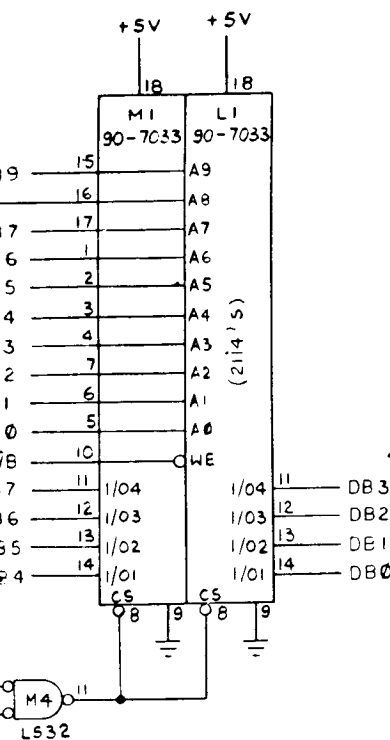
Sheet 1, Side B
ASTEROIDS DELUXE™
Microprocessor
Section of 036471-02 C



AM8304 B INSTEAD OF 74LS245.

RAM,		
6000		1
6800		1
7000		1
7800		1

HIGH SCORE CIRCUITRY



temporary storage space for
led when ZPAGE (Zero
When R/WB (from the
stores the data byte in-
the location addressed
us (AB0 thru AB7). When
J reads the stored data
location.

, when low, has the ef-
es 2 and 3 within the
ater programming flex-

ter is disabled by RESET. During Self-Test, the NMI
y TEST.

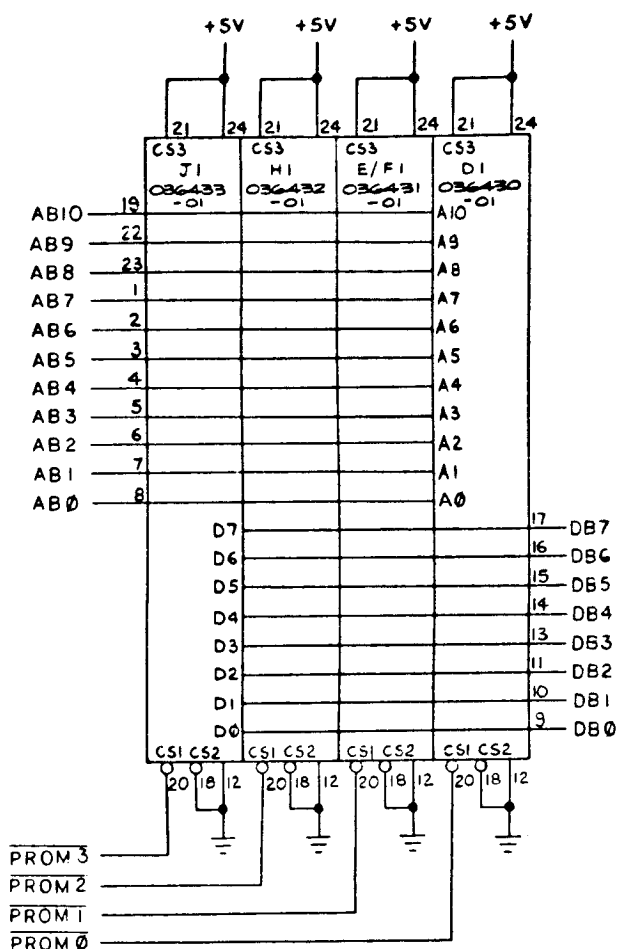
NOTE:
Either a 74LS245 or an AM8304B may be used at
location E2. Pin numbers not enclosed in paren-
theses are for 74LS245. Pin numbers in paren-
theses are for an AM8304B.



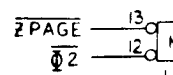
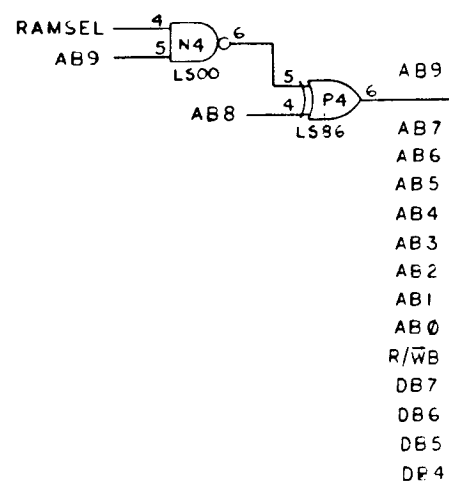
ROM/PROM CIRCUITRY

FROM SWITCH INPUTS
SHEET 2, SIDE B

Program memory for the Asteroids Deluxe™
game is contained in three ROMs.



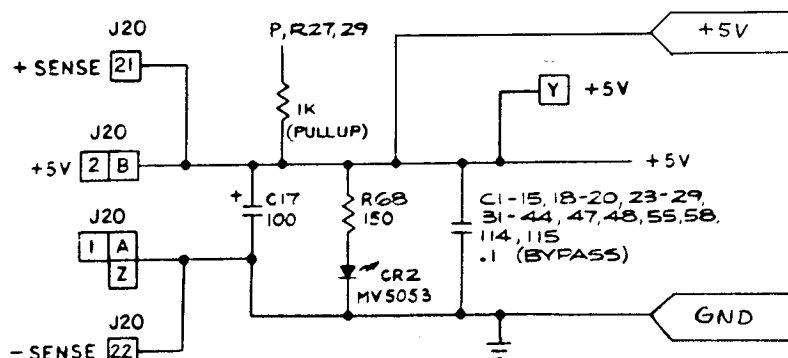
RAM CIRCUITRY



The RAM is the temporary memory used by the MPU and is enabled when the Page enable (PE) is low. When the PE (MPU) is low, the RAM stores the output (DB0 thru DB7) at the address selected by the MPU address bus (AB0-AB9). When R/WB is high, the MPU reads a byte at the addressed location.

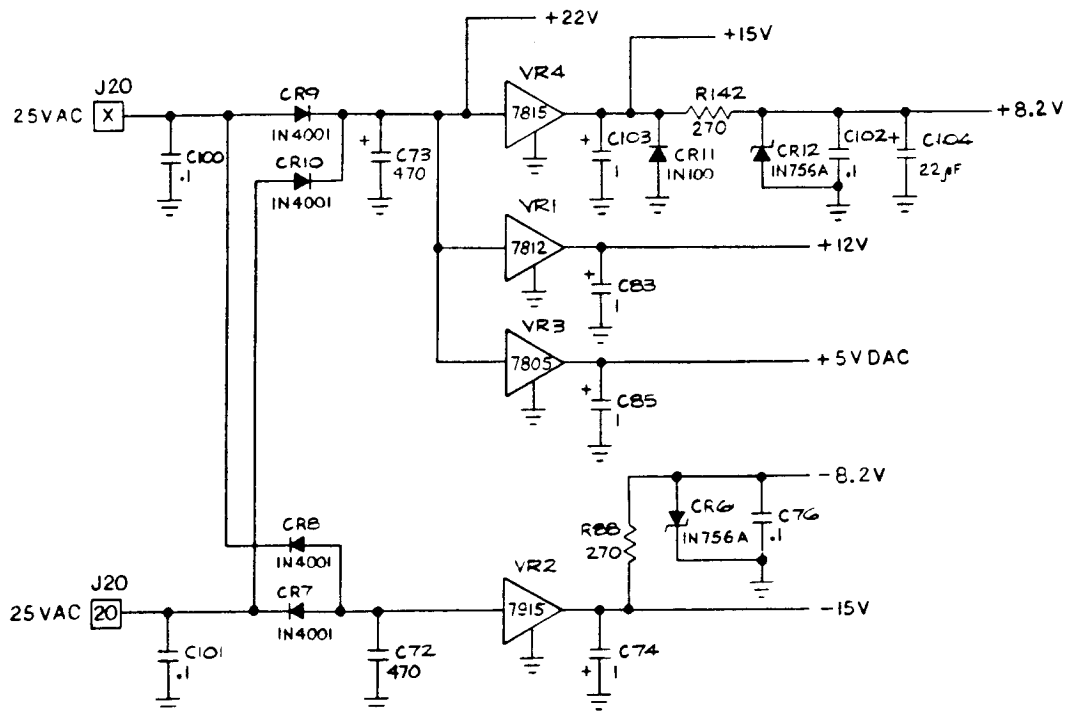
The signal RAMSEL, which is the effect of swapping pages, is used to select RAM. This allows greater flexibility.

POWER INPUT



This circuitry consists of the PCB inputs and outputs for the + 5 VDC logic power and 25 VAC input to the on board regulators. The + 5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

The 25 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR8 rectify the negative cycle of the input and the 7915 regulates the voltage at -15 VDC. Diodes CR9 and CR10 rectify the positive pulse of the 25 VAC input and the 7815 regulates the voltage at + 15 VDC. The 7812 regulates at + 12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR12 supplies the + 8.2 VDC for the sample and hold circuit. The + 22V (unregulated) is used to power operational amplifiers P1 and L8 in the audio output.

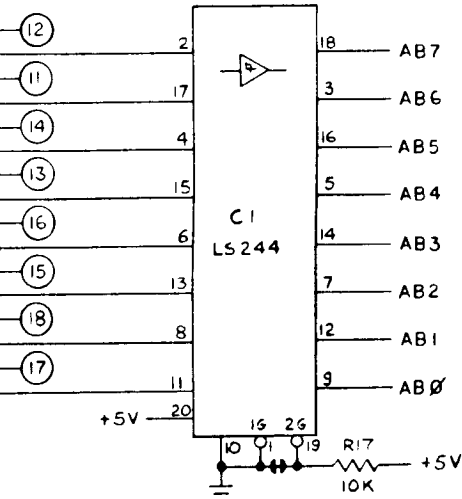
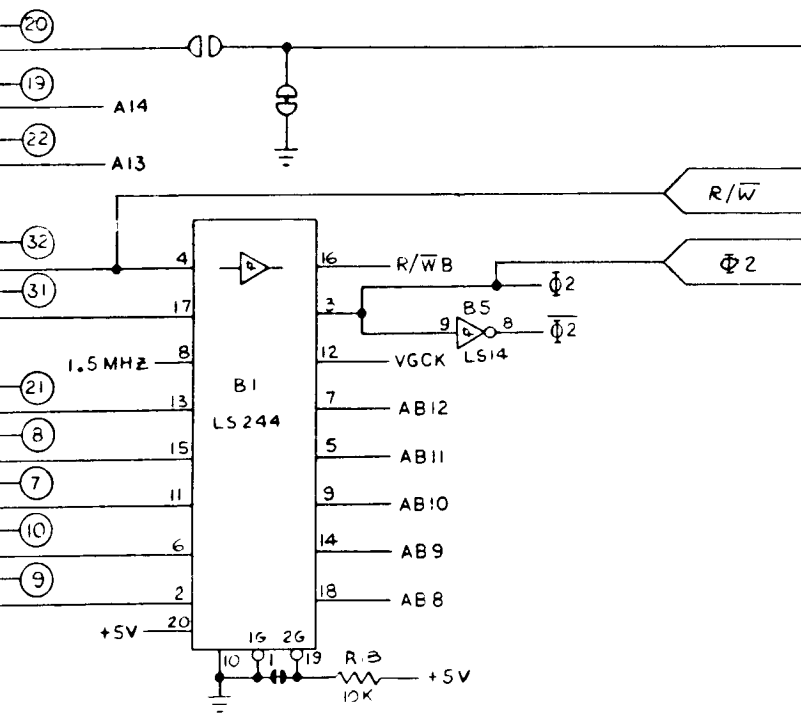


Denotes a test point

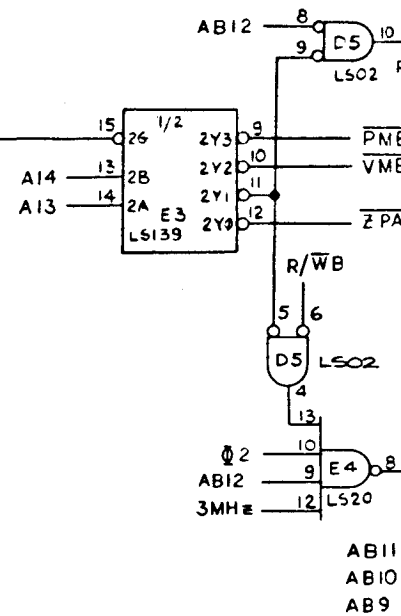
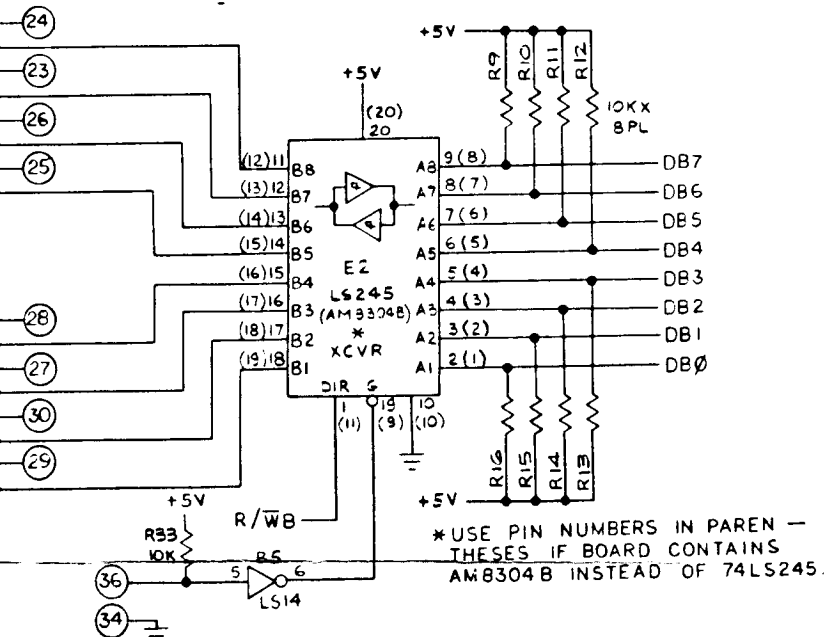
ADDRESS																DATA								FUNCTION
A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0																				Scratch RAM
0	1	0	0	0								0	0	0	R									Not used
0	1	0	0	0								0	0	1	R	D								3 KHz
0	1	0	0	0								0	1	0	R	D								VG halted
0	1	0	0	0								0	1	1	R	D								Shield switch
0	1	0	0	0								1	0	0	R	D								Fire switch
0	1	0	0	0								1	1	0	R	D								Slam switch
0	1	0	0	0								1	1	1	R	D								Self-test switch
0	1	0	0	1								0	0	0	R	D								Left coin switch
0	1	0	0	1								0	0	1	R	D								Center coin switch
0	1	0	0	1								0	1	0	R	D								Right coin switch
0	1	0	0	1								0	1	1	R	D								1-player start switch
0	1	0	0	1								1	0	0	R	D								2-player start switch
0	1	0	0	1								1	0	1	R	D								Thrust switch
0	1	0	0	1								1	1	0	R	D								Rotate right switch
0	1	0	0	1								1	1	1	R	D								Rotate left switch
0	1	0	1	0									0	0	R							D	D	Option switch 8, 7 (at R5)
0	1	0	1	0									0	1	R							D	D	Option switch 6, 5
0	1	0	1	0									1	0	R							D	D	Option switch 4, 3
0	1	0	1	0									1	1	R							D	D	Option switch 2, 1
0	1	0	1	1				0			A	A	A	A	R									POKEY
0	1	0	1	1				1			A	A	A	A	R									EAROM read
0	1	1	0	0	0						A	A	A	A	W									Start VG
0	1	1	0	0	1						A	A	A	A	W	D	D	D	D	D	D	D	D	Latch EA address/data
0	1	1	0	1	0										W									Watchdog reset
0	1	1	0	1	1										W	D	D							Explosion pitch
0	1	1	0	1	1										W			D	D	D	D			Explosion volume
0	1	1	1	0	0										W									3800 VG reset
0	1	1	1	0	1										W						D	D		EA control latch
0	1	1	1	1	0							0	0	0	W									1-player start LED
0	1	1	1	1	1	0						0	0	1		D								2-player start LED
0	1	1	1	1	1	0						0	1	0		D								Not used
0	1	1	1	1	1	0						0	1	1		D								Ship thrust sound
0	1	1	1	1	1	0						1	0	0		D								Bank select
0	1	1	1	1	1	0						1	0	1		D								Left coin counter
0	1	1	1	1	1	0						1	1	0		D								Center coin counter
0	1	1	1	1	1	0						1	1	1		D								Right coin counter
0	1	1	1	1	1	1																		Noise generator reset
1	0	0	0	0	0																			Vector RAM
1	0	0	0	0	1																			Vector RAM
1	0	0	1												R									Vector ROM
1	0	1	0												R									Vector ROM
1	1	0	0	0																				Program ROM
1	1	0	1												R									Program ROM

ADDRESS DECODING

NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes.



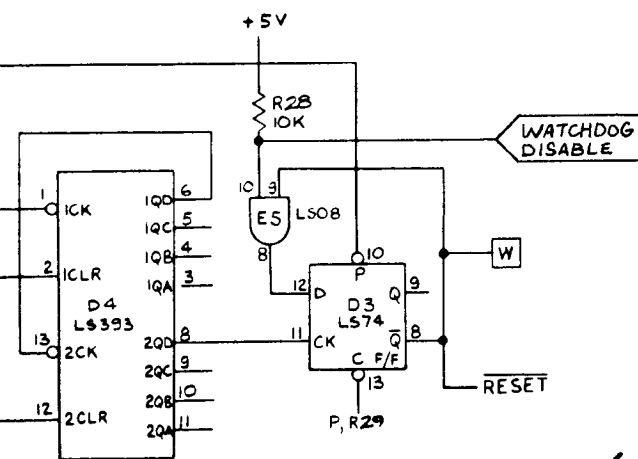
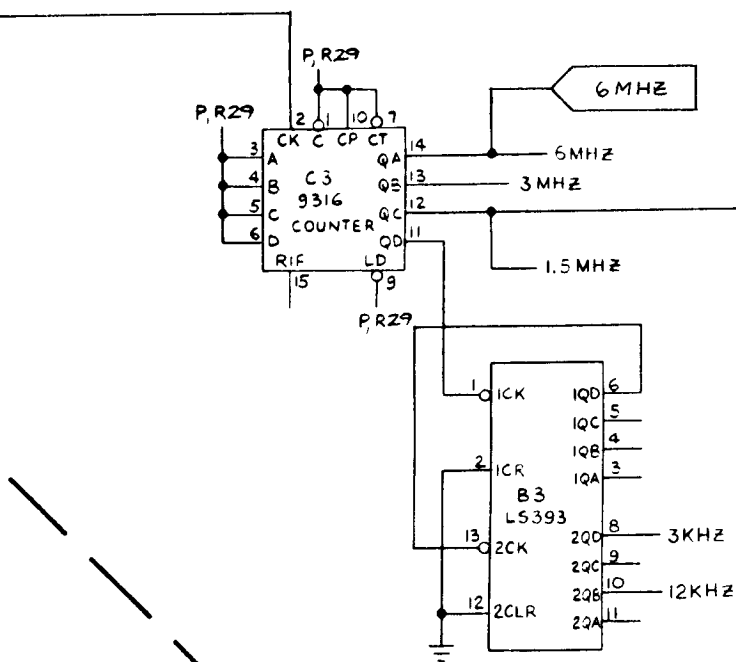
NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes. If a 74LS244 is installed at location B1 and/or C1, the split pad for that location should be filled with solder. If a 74LS241 is used, the appropriate split pad should be open.



	HEXADECIMAL	A15 A14
INPUTS	0-3FF	0
	2000	0
	2001	0
	2002	0
	2003	0
	2004	0
	2006	0
	2007	0
	2400	0
	2401	0
	2402	0
	2403	0
	2404	0
	2405	0
2406	0	
2407	0	
2800	0	
2801	0	
2802	0	
2803	0	
OUTPUTS	2000	0
	2C40	0
	3000	0
	3200	0
	3400	0
	3600	0
	3600	0
	3800	0
	3A00	0
	3C00	0
	3C01	0
	3C02	0
	3C03	0
	3C04	0
3C05	0	
3C06	0	
3C07	0	
3E00	0	
RAM, ROM	4000	1
	4400	1
	4800	1
	5000	1
	6000	1
	6800	1
7000	1	

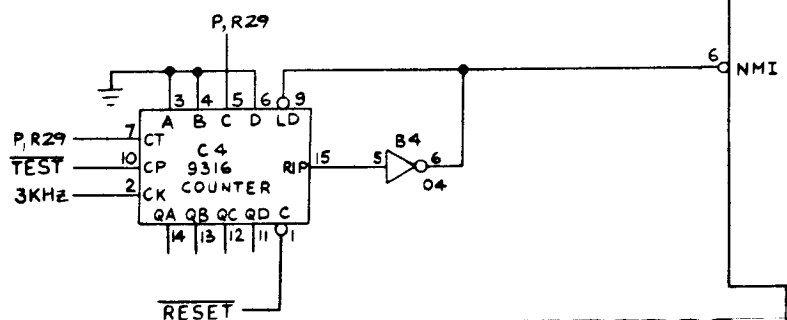
MPU CIRCUITRY

of crystal Y1 and associated in-
B3. Counters C3 and B3 count the
he frequencies necessary for the



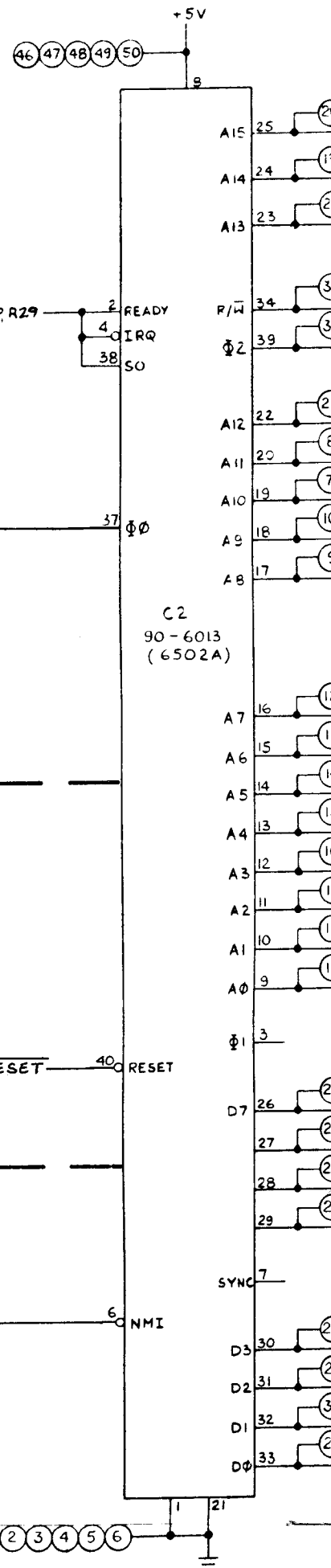
COUNTER

(non-maskable interrupt) counter causes an interrupt
out of the MPU every 4 msec. The interrupt is derived
KHz by a factor of 12 through counter C4. The inter-
when pin 6 of inverter B4 goes low. During power-up,
ter is disabled by RESET. During Self-Test, the NMI
y TEST.



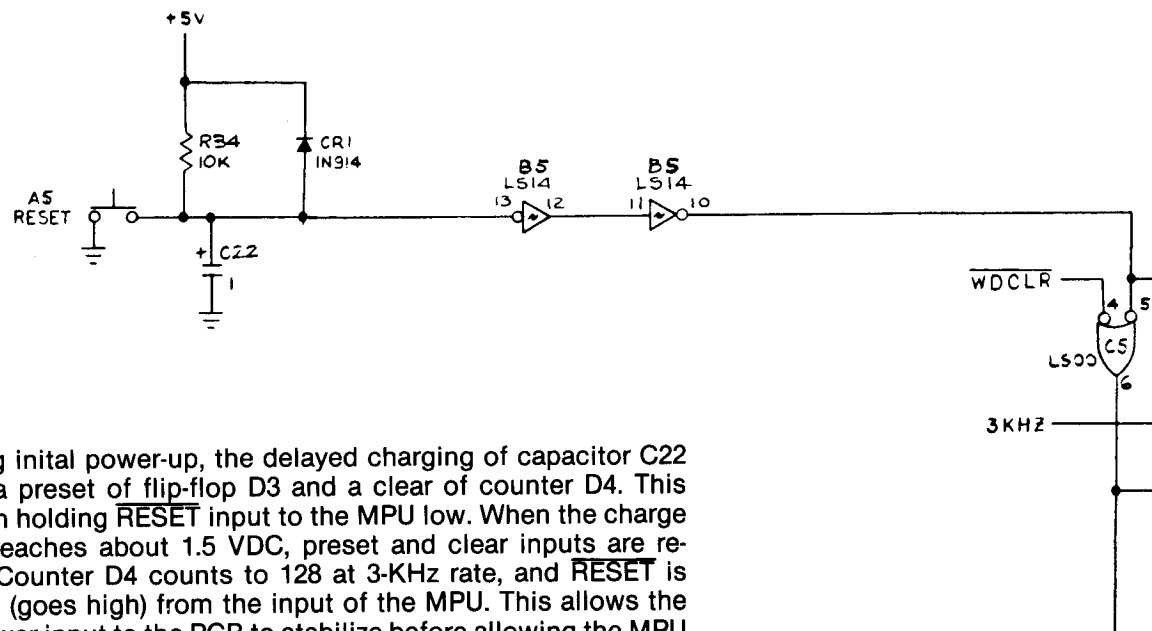
NOTE:

Either a 74LS245 or an AM8304B may be used at
F2. Pin numbers not enclosed in paren-



NOTE:

POWER RESET AND WATCHDOG COUNTER



During initial power-up, the delayed charging of capacitor C22 causes a preset of flip-flop D3 and a clear of counter D4. This results in holding RESET input to the MPU low. When the charge of C22 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D4 counts to 128 at 3-KHz rate, and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter D4 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter D4 will count up to the RESET state and cause the MPU to return to its initialization routine.

NMI CC

The NMI (non-maskable interrupt) at the NMI input is generated by dividing 3 by the number of interrupt occurs while the NMI counter is disabled by



Denotes a test point