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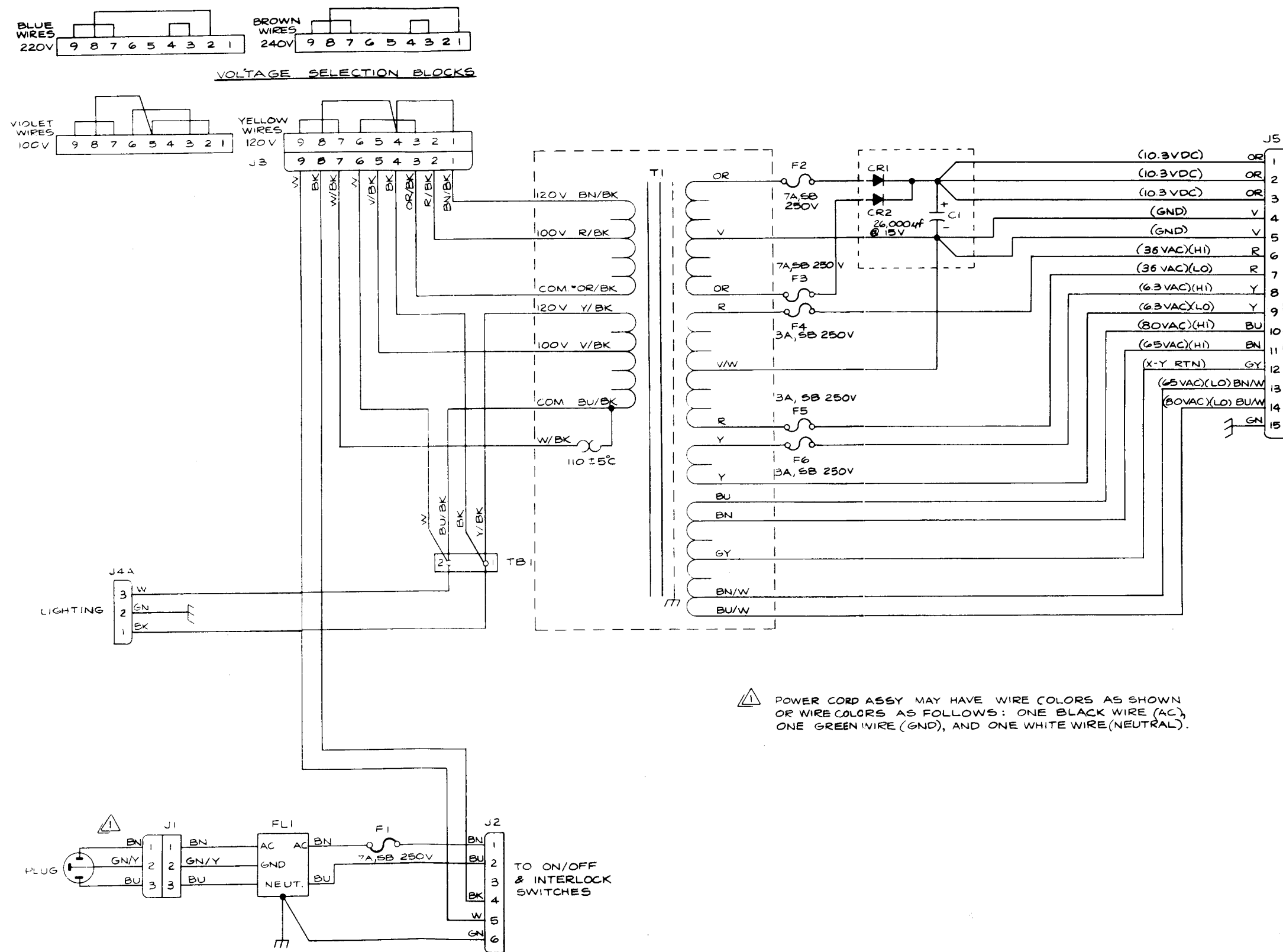


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VIDEO POWER SUPPLY WIRING DIAGRAM (034633-01 A)



POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND), AND ONE WHITE WIRE (NEUTRAL).

REGULATOR/AUDIO PCB SCHEMATIC

Regulator/Audio PCB 034485-01 A

The Regulator/Audio PCB has the dual function of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through the sense inputs +SENSE and -SENSE. The input is directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage to the game PCB. This eliminates a reduced voltage due to a voltage drop on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the voltage on the game PCB. Once adjusted, the voltage at the game PCB will remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between +5 V and GND test point of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND test point of Regulator/Audio PCB and plus lead to +5 V REG test point of game PCB. Note the voltage reading. If greater than +5.5 VDC, try cleaning the connectors on both the game PCB and Regulator/Audio PCB.
4. If cleaning PCB edge connectors doesn't drop the voltage difference, connect minus lead of voltmeter to GND test point of game PCB and plus lead to +5 V REG test point of Regulator/Audio PCB and plus lead to +5 V REG test point of game PCB. From this you can see if the harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA1584Q audio amplifier with a gain of ten. In Asteroids, the audio is permanently on. Therefore, this audio circuit is always on, even when the game is in the attract mode.

The audio circuit is repeated on Sheet 2, Side B, for more information about its operation.

Drawing Package Supplement

to

ASTEROIDS

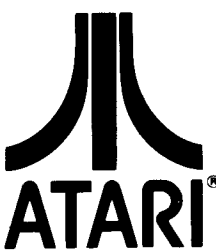
Operation, Maintenance, and Service Manual

Contents of this Drawing Package

Game Wiring Diagram, Coin Door and Power Supply
Microprocessor
Video Generator
Switch Inputs, Coin Counter, LED and Audio Outputs

Sheet 1, Side A
Sheet 1, Side B
Sheet 2, Side A
Sheet 2, Side B

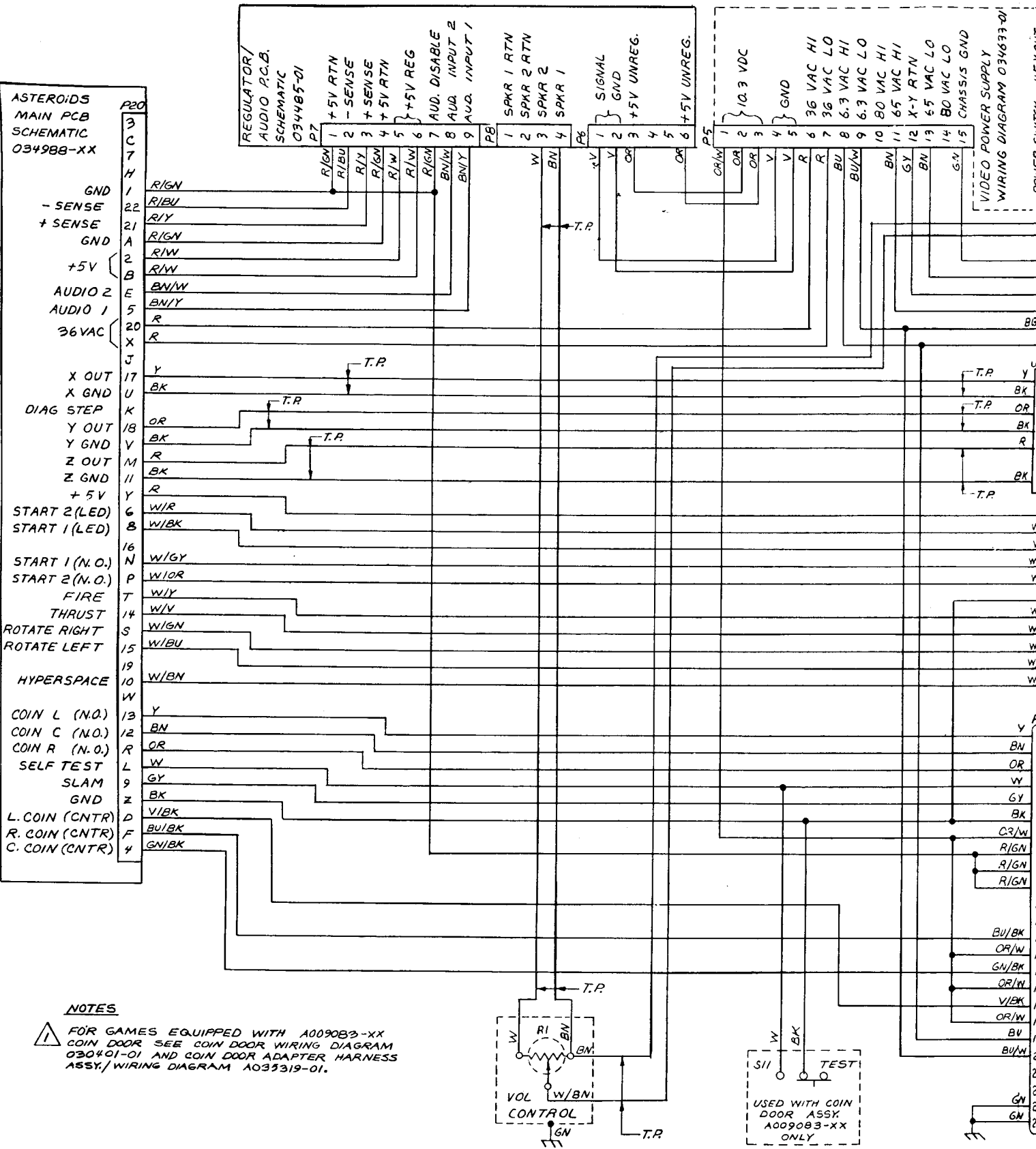
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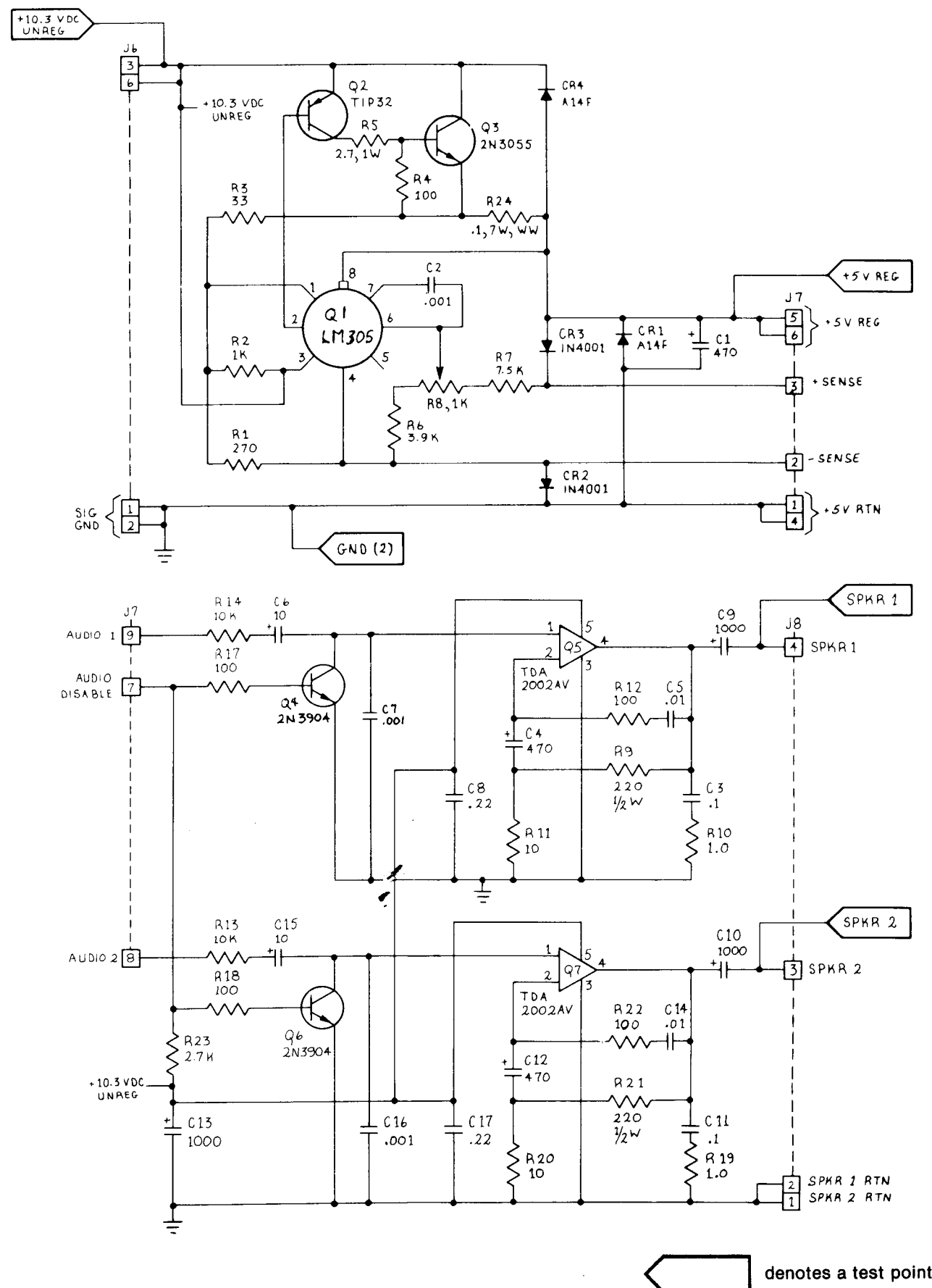
ASTEROIDS WIRING DIAGRAM (035156-01 B)



NOTES
FOR GAMES EQUIPPED WITH A009083-XX COIN DOOR SEE COIN DOOR WIRING DIAGRAM 0350401-01 AND COIN DOOR ADAPTER HARNESS ASSY/WIRING DIAGRAM A035319-01.

USED WITH COIN DOOR ASSY A009083-XX ONLY

B, including



SLAM SWITCH

GY BU

BU

BU

R

GN/R

BK/OR

OR/BK

OR

BK/Y

Y/BK

Y

GY

GY

BN

GN

BN/BK

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

15 POS MOLEX
PLUG + MALE
TERMINALS

COIN COLOUNTER

COIN SWITCH #1
(RIGHT)

COIN SWITCH #2
(LEFT)

LOCKOUT COIL

BN

BK/Y

V/BK

Y

OC

ONC

OC

ONC

OC

ONC

BN/BK

BN

GN

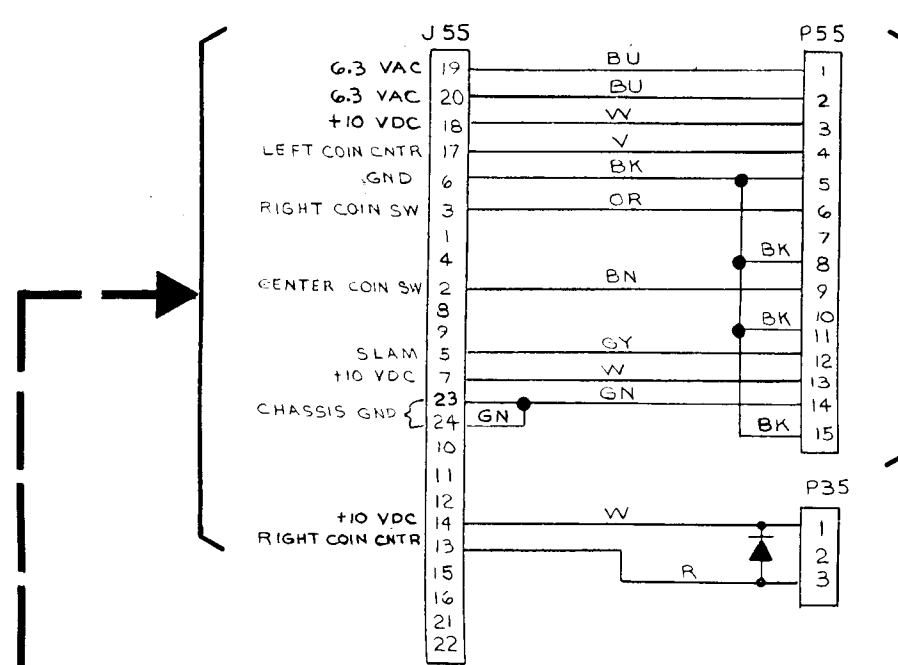
BN/BK

COIN #2
(LEFT)

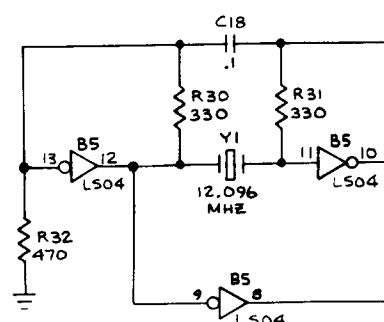
COIN #1
(RIGHT)

FRONT VIEW
OF COIN DOOR

COIN DOOR ADAPTER HARNESS

[illegible]

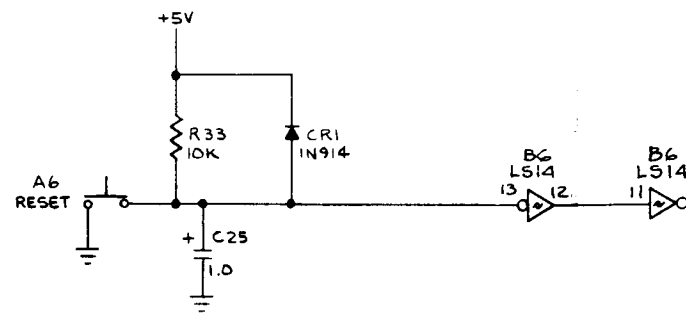
CLOCK CIRCUIT



NOTE:
THE MPU IN THIS GAME OPERATES AT A FREQUENCY
OF 1.5 MHZ. THEREFORE THE MPU CHIP MUST BE
6502A. THE 6502'S MAXIMUM FREQUENCY IS 1 MHZ
AND IS NOT COMPATIBLE WITH THIS GAME.

The clock circuit consists of crystal Y1 and associated inverters and counters C4 and B4. Counters C4 and B4 count the crystal frequency down to the frequencies necessary for the Asteroids game.

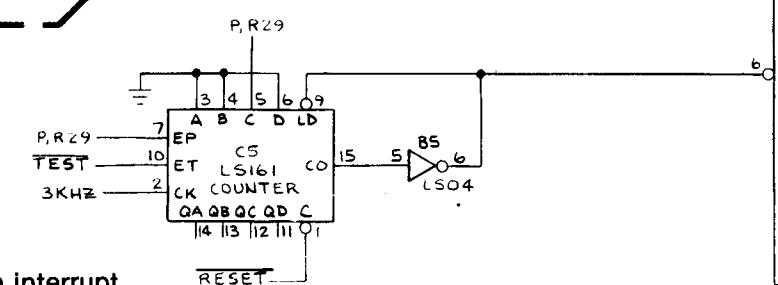
POWER RESET AND WATCHDOG COUNTER



During initial power-up, the delayed charging of capacitor C25 causes a preset of flip-flop D4 and a clear of counter D5. This results in holding RESET input to the MPU low. When the charge of C25 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D5 counts to 128 at 3 KHz rate and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter D5 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter D5 will count up to the RESET state and cause the MPU to return to its initialization routine.

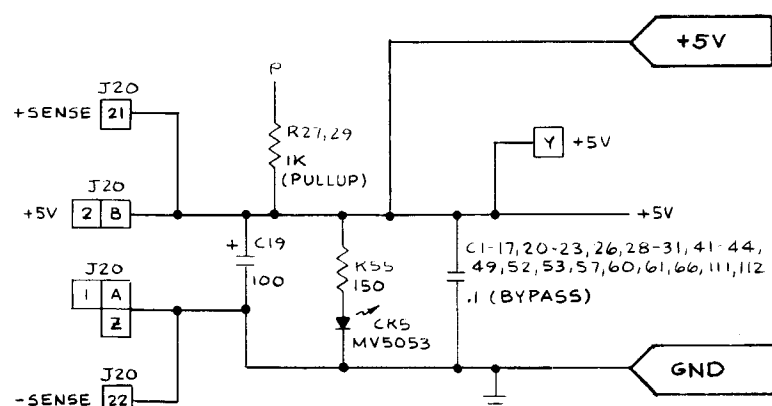
NMI COUNTER



The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C5. The interrupt occurs when pin 6 of inverter B5 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

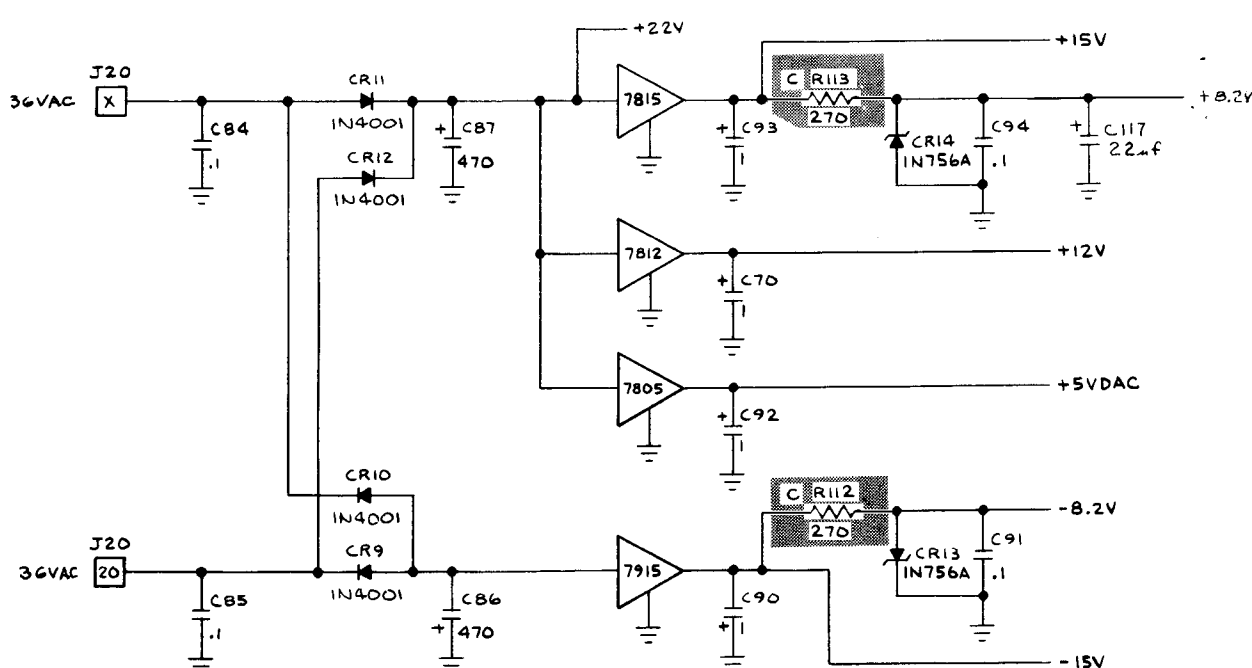
denotes change by indicated revision
denotes a test point

POWER INPUT



This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and 36 VAC input to the on board regulators. The +5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

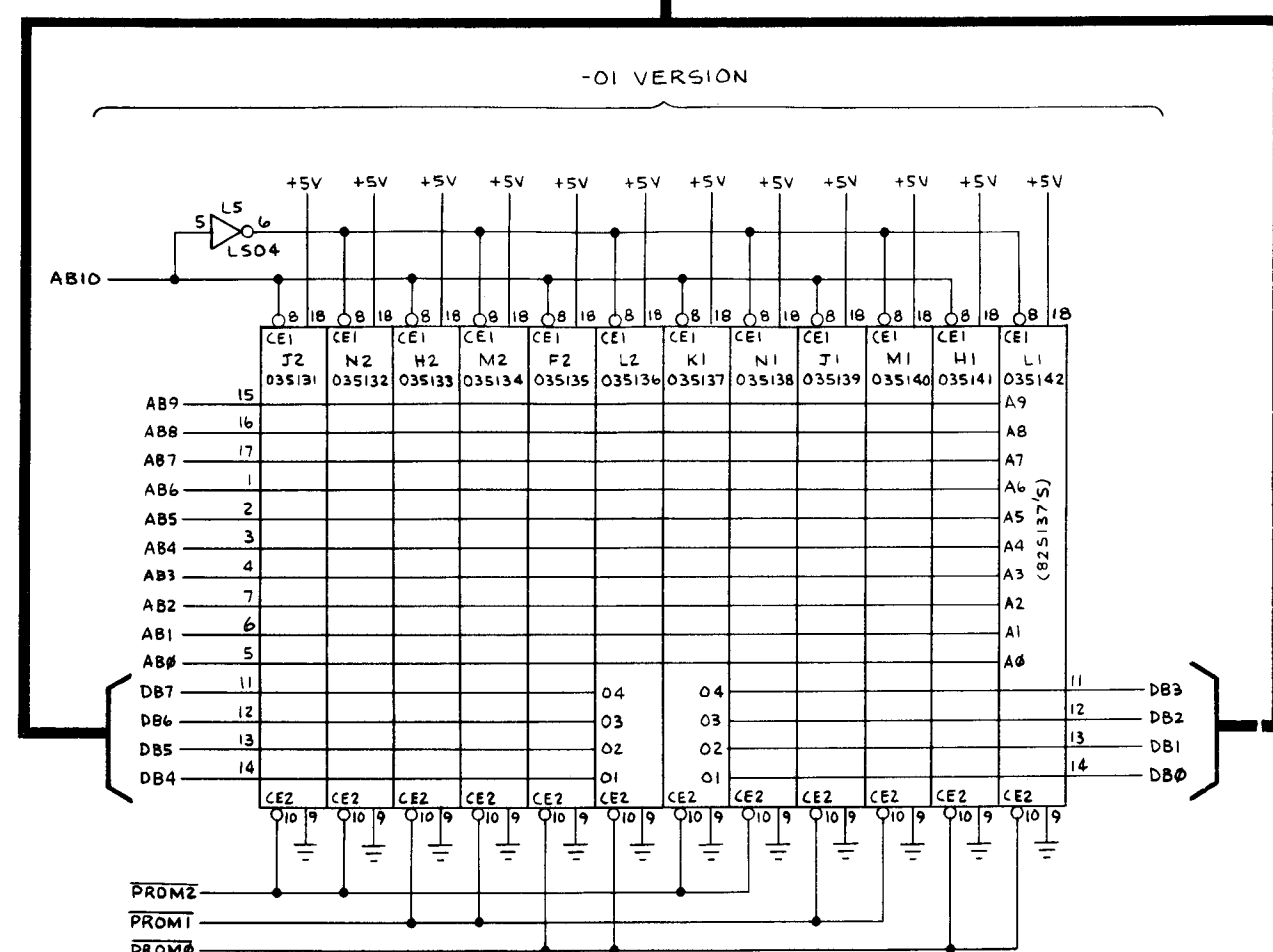
The 36 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR10 rectify the negative cycle of the input and the 7915 regulates the voltage at -15 VDC. Diodes CR11 and CR12 rectify the positive pulse of the 36 VAC input and the 7815 regulates the voltage at +15 VDC. The 7812 regulates at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR14 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) amplifier P11 and L8 in the audio output.



FROM SWITCH INPUTS SHEET 2, SIDE B

ROM/PROM CIRCUITRY

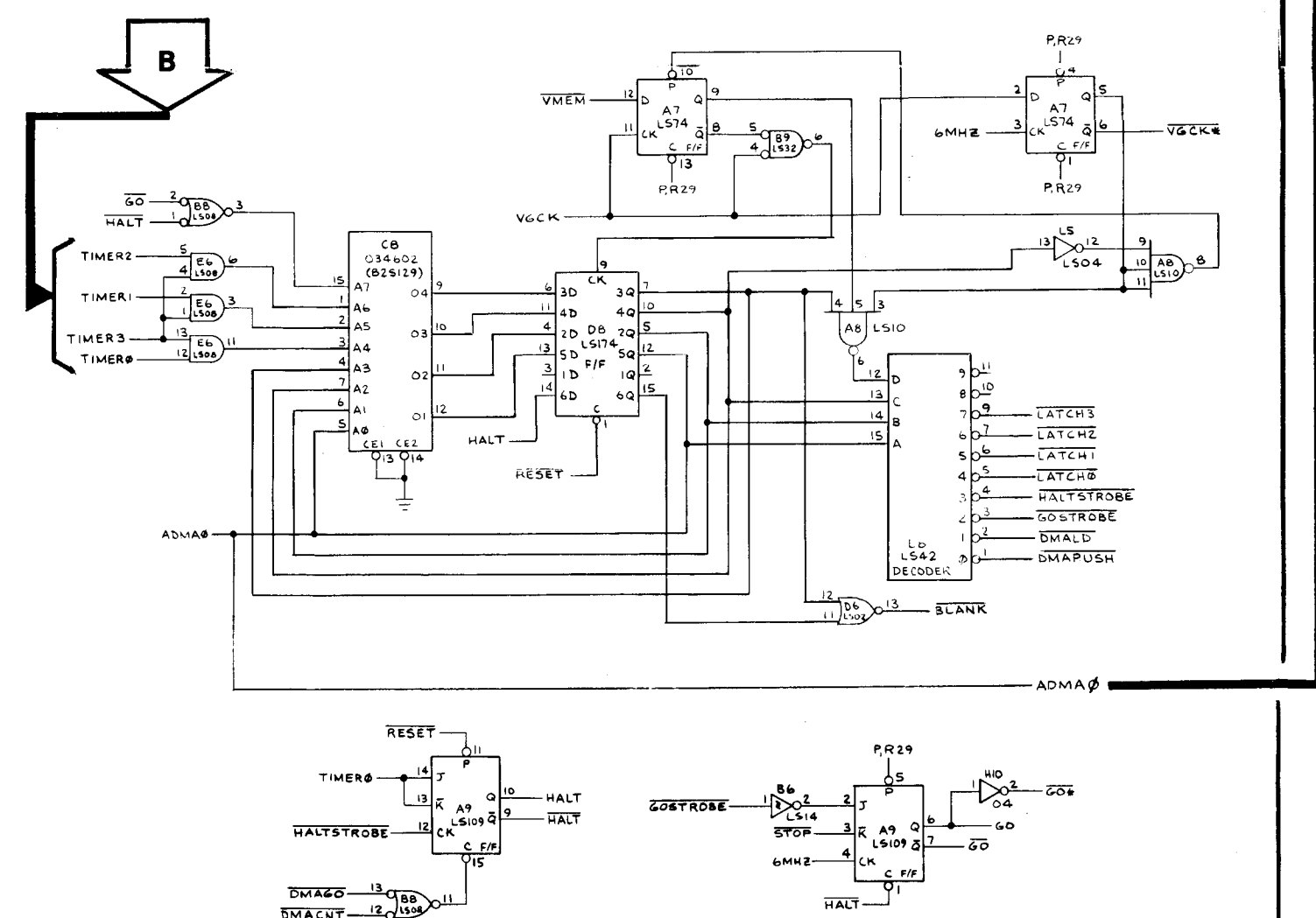
Program Memory for the Asteroids is contained in PROMs for the -01 version ROMs for the -02 version of the PCB equivalent to four PROMs. All PROMs a common enable must be removed with a ROM. For example, remove locations F2, H1, L2 and L1 before ROM at location F1.



[illegible]

The program counter may also be preset to “jump” to a new address. This new address can be loaded into the program counter from the vector generator memory via

The program counter may also be preset to “return” to a previous address which it had stored in its “stack”. The stack consists of register files F4, H4, J4, and down/up counter K5. The stack is a 4-word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when DMAPUSH is low. Immediately after information is written into the stack, counter K5 increments one count. Immediately before loading the program counter from the stack, counter K5 decrements one count.



The state machine is the “master controller” of the vector generator circuitry. It receives instructions from the game MPU, via the vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector generator ROM memory, using the vector generator program counter to do so. The state machine reads the vector generator ROM data (via Timer 0-3) and decodes this information to determine how it should use this data: 1) to draw a vector; 2) to move the monitor beam to a new position on the monitor display; 3) to “jump” to a new vector memory address; 4) to return to a previous vector memory address; or 5) to tell the game MPU that it has completed its current instructions, and is waiting for its next command.

During initial power-up of the game, the HALT signal is preset low. The microcomputer reads the high HALT signal through its switch input port (buffer M10) on data line DB0. This tells the microcomputer that the vector generator is halted and waiting for an instruction. To ensure that the beam is off when the state machine is halted, the high HALT, clock-

The VGCK input to the clock circuitry is a buffered 1.5 MHz clock signal from the microcomputer. This is the same frequency used to clock the MPU of the microcomputer. The signal clocks latch D8 unless the microcomputer is addressing the vector RAM or ROM memories (when VMEM goes low). Then the clock input to latch D8 goes high and stays high until VMEM goes high.

[illegible]

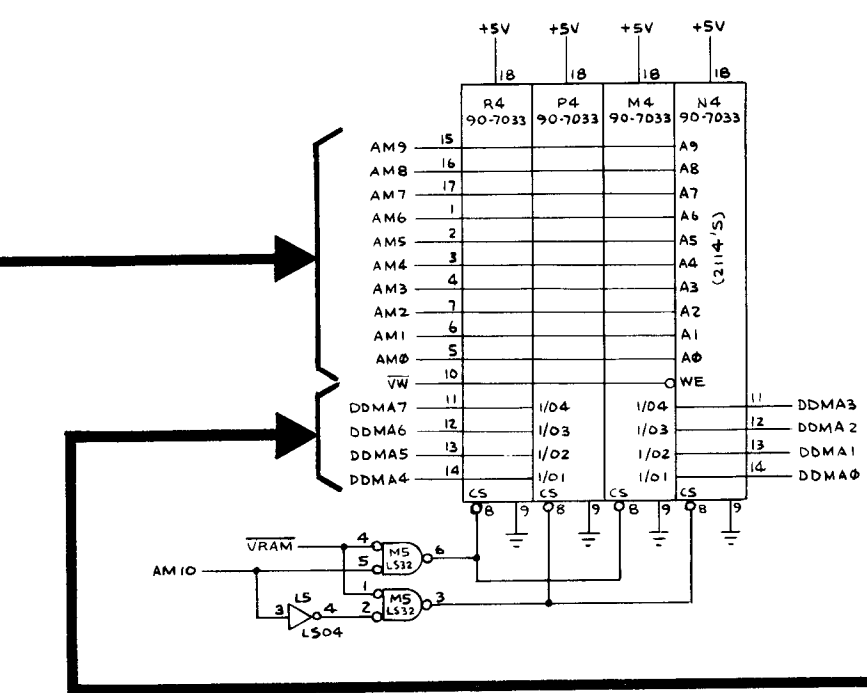
This address-selecting arrangement allows the game MPU to access the vector generator memory, i.e., write data into the vector generator RAM to instruct the vector generator what it should do next. The address selector can then allow the vector generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.

The purpose of the vector timer is to time out the length of time it takes to "draw" an actual vector on the monitor display. During the interval when the X and Y position counters are actually drawing the

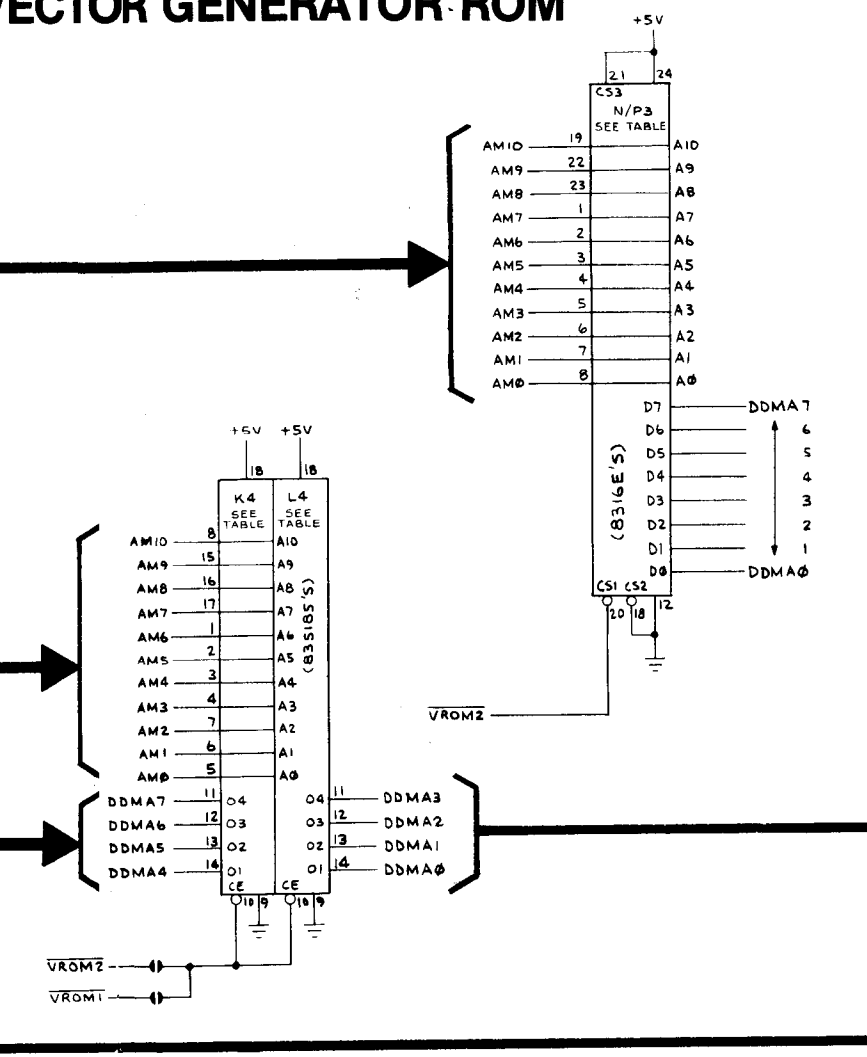
If the TIMER signals are all high, ALPHANUM goes low and data signals DVX11 and DVI11 are decoded by decoder E7. This is added to the scale factor and loaded into the counters.

The state machine can preset these counter number from their previous content beam to "jump" to a new location on the tape simultaneously, i.e., for drawing a new vector position than where the previous vector ended.

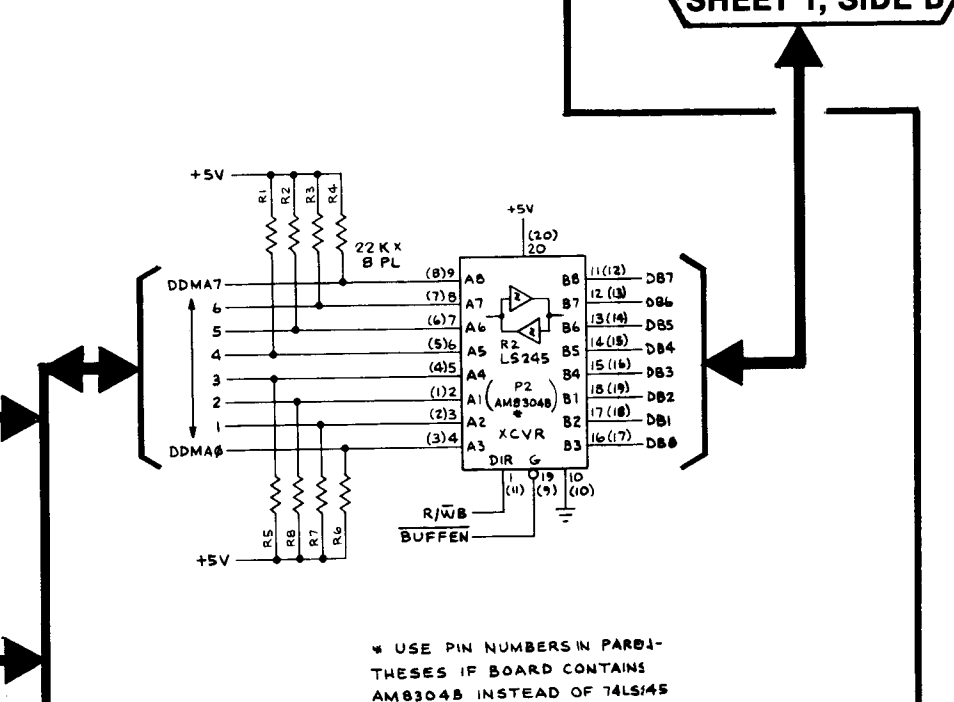
VECTOR GENERATOR RAM



VECTOR GENERATOR ROM



VECTOR GENERATOR DATA BUFFER



* USE PIN NUMBERS IN PARD-
THESES IF BOARD CONTAINS
AM9304B INSTEAD OF 74LS145

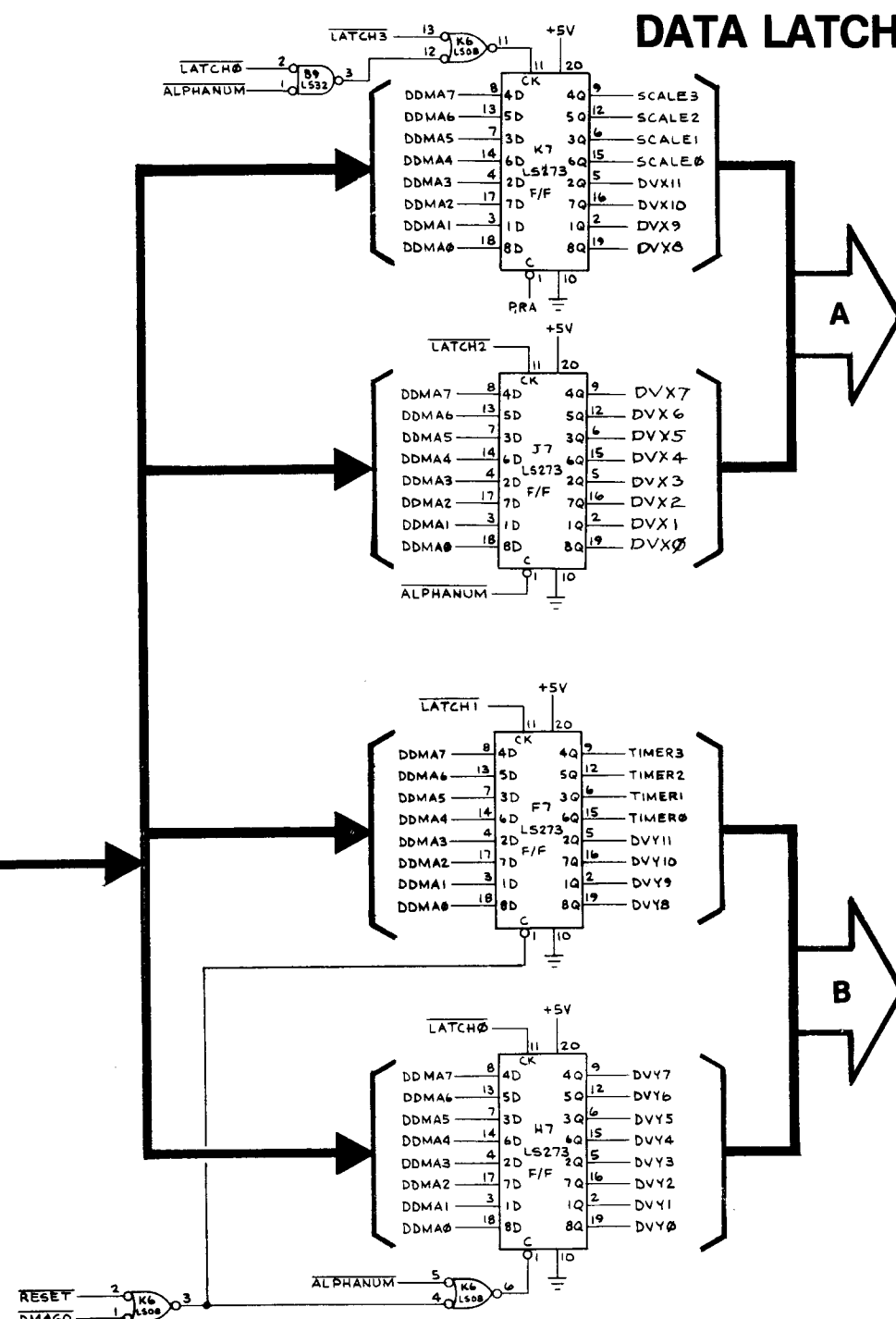
ROM #	LOC	PROM #	LOC	ATKAL
035127	W/P3	035130	L4	
R3			L4	

The vector generator memory consists of 2K of RAM and 4K of ROM. It may be directly accessed by the MPU of the microcomputer through the direct memory access process (DMA). Data is written in from the microcomputer thru data buffer R2 when BUFFEN and R/WB are low.

The 2kx8 vector generator program memory chip N/P3 may be substituted with two equivalent 1Kx8 chips in location K4 and L4.

denotes change by indicated revision

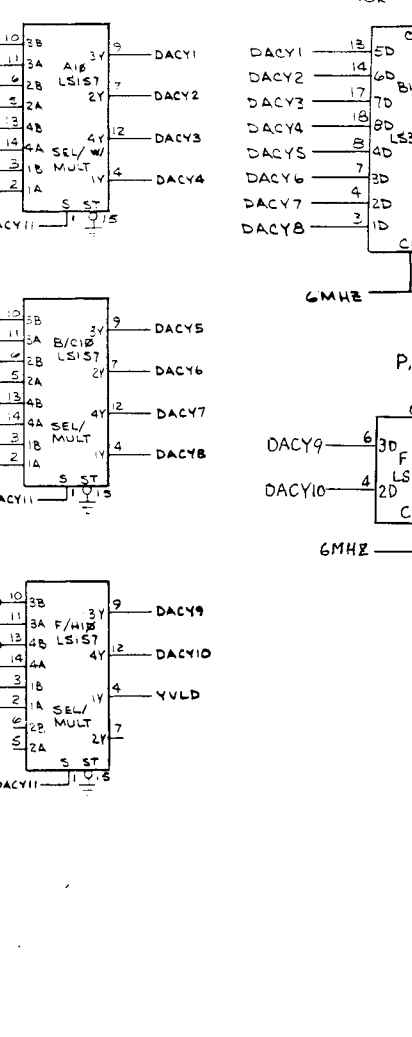
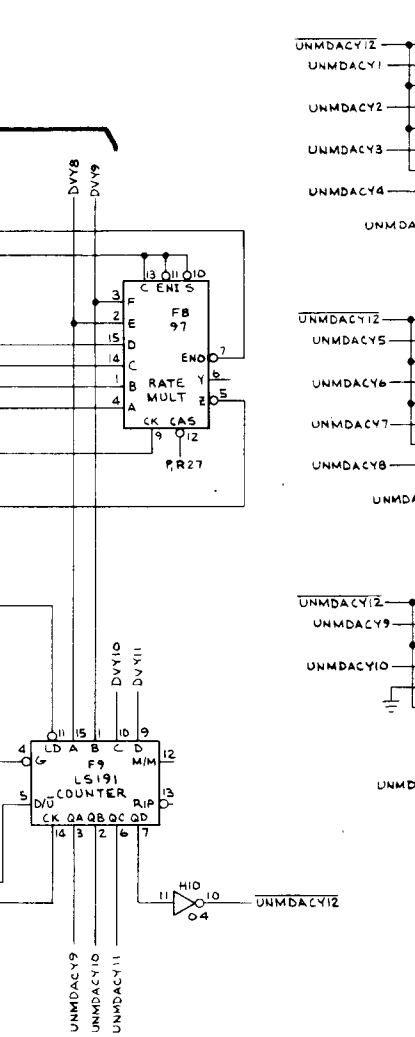
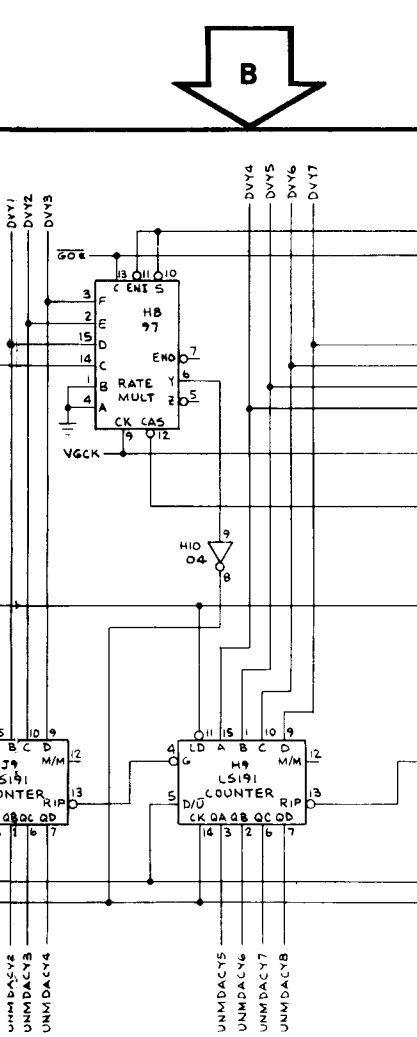
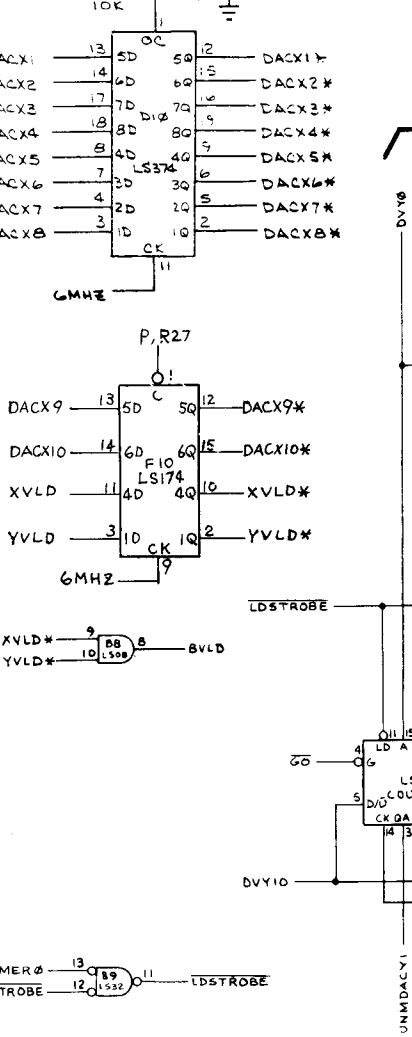
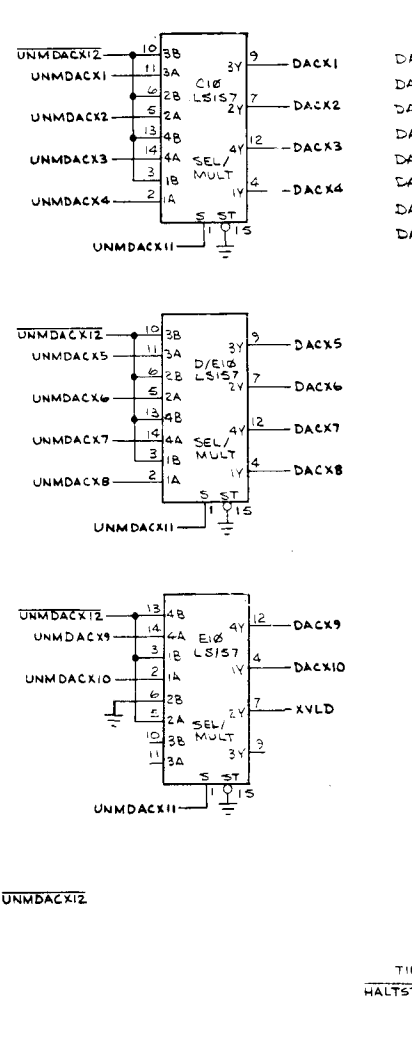
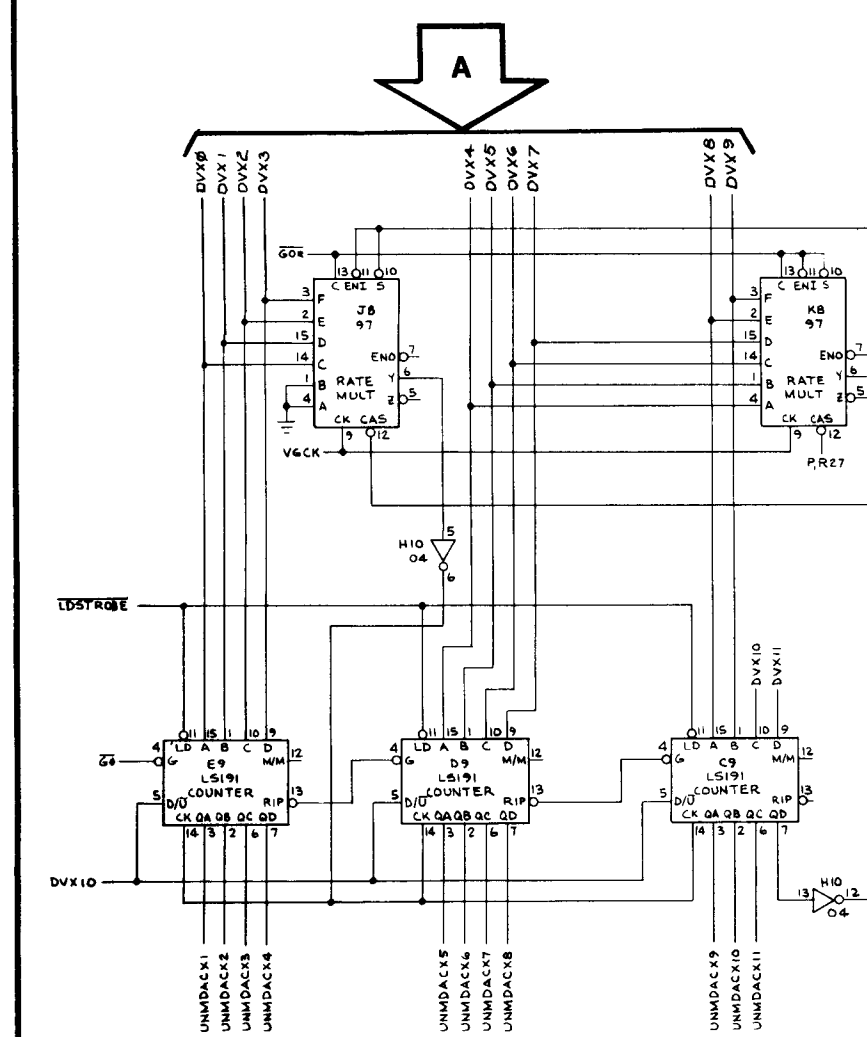
VECTOR GENERATOR MEMORY DATA LATCHES



The data latches consist of latch 0 (H7), latch 1 (F7), latch 2 (J7), and latch 3 (K7). Inputs DDMA0 thru DDMA7 are the data outputs from the vector generator memory.

Latches 0 thru 2 are directly clocked by the rising edge of the LATCH0, LATCH1, and LATCH2 outputs from the vector generator's state machine. Latch 3 is clocked by LATCH3 or by LATCH0, if ALPHANUM is low. Latch 0 is cleared when RESET, DMAGO, or ALPHANUM goes low. Latch 1 is cleared by ALPHANUM.

X AND Y POSITION COUNTERS



"jumping" to this new position, the beam itself is turned off to prevent unwanted lines from appearing on the screen. To preset this new position into the counters, the state generator causes LDSTROBE to go low. At this time, a new 12-bit number (DVX0-11) is loaded into the counters from the vector generator memory data latches.

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific distance relative to where it was. During this beam movement, the beam is turned on with the desired intensity. This is the procedure used to draw a vector on the monitor screen. The direction (to the left or right) and length (0 to 1023) of the vector to be drawn relative to the beam's current position is determined by DVX0-11 (from the vector generator memory data latches). This data contains information that determines how many clock pulses the counters will receive and whether the counters will count up or down.

DVX0-9 memory data is loaded into rate multipliers J8 and K8. The function of these devices is to space the desired number of counter clock pulses at equal intervals over the time period that it will take to draw the desired vector. This insures that vectors of different lengths will still be displayed with the same relative beam intensity. DVX10 and 11 are loaded directly into the counters. DVX10

determines whether the counters count up or down. DVX11 is used to control the select input of multiplexers D10, E10, and F10.

The UNMDACK1 thru UNMDACK10 (X axis unmultiplexed digital-to-analog converter signals) are transferred to the output of the multiplexers and stored at the outputs of the latches on each rising edge of the 6 MHz clock (from the microcomputer clock circuitry). The DAC1* thru DAC10* signals are sent to the digital-to-analog converters (DACs) in the X video output.

The DAC1* thru DAC10* outputs represent the physical placement of the beam on the monitor. The far left of the monitor screen is 0, the center is 512, and the far right is 1023. Therefore, if the DAC1* thru DAC10* signal was greater than 1023, the monitor beam would go off the right side of the screen and start again on the left side of the screen, a "wraparound" condition. To prevent a wraparound, the multiplexers' select input from UNMDACK11 goes high when the count is greater than 1023 or less than 0. This selects UNMDACK12 to be output from the multiplexers to the DACs, forcing all zeros or all ones, and thus keeping the beam on the appropriate side on the screen, instead of allowing it to wraparound.

The XVLD and YVLD (X and Y valid) outputs from the X and Y position counter multiplexers are latched and gated together to enable the Z axis output, BVLD (beam valid).

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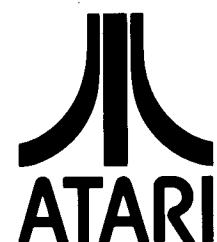
Sheet 2, Side A

ASTEROIDS

Video Generator

Section of 034986-XX

F

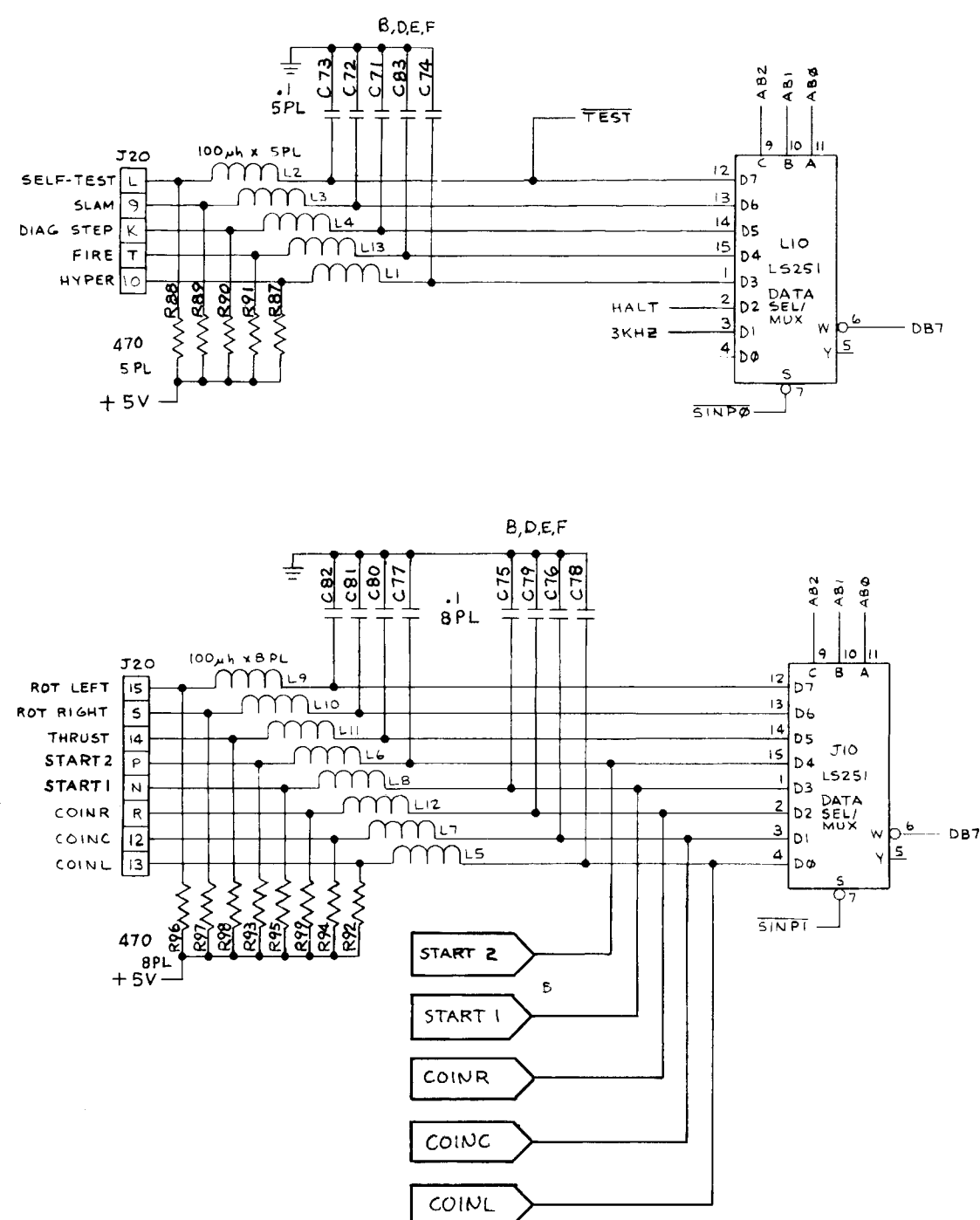


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INPUTS

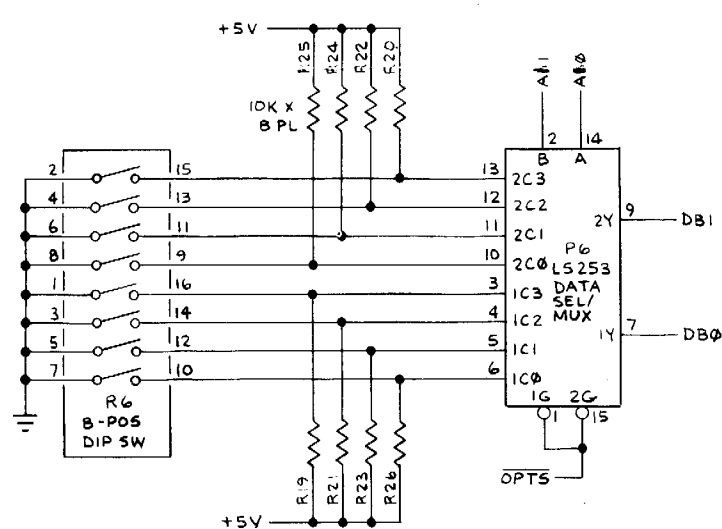
PLAYER INPUT CIRCUITRY



DIAG STEP (diagnostic step), 3 KHz, SELF-TEST SLAM, HALT, FIRE and HYPER inputs are read by the MPU when SINP0 (switch input zero enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on DB7. Switch inputs are active when pulled to ground. DIAG STEP, 3 KHz, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the antislam switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.

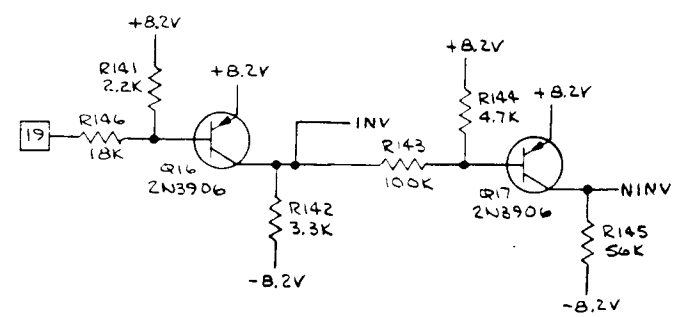
The coin door and some control panel switches are read by the MPU when SINP1 (switch input one enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on data line DB7. Switch inputs are "on" when pulled to ground.

OPTIONS INPUT CIRCUITRY



The game option switches are read by the MPU when OPTS (option switch enable) is low. Switch toggles to be read are selected by AB0 and AB1 from the MPU. Switch toggles 1, 3, 5, and 7 are read on data line DB0 and toggles 2, 4, 6 and 8 are read on DB1. Toggle inputs are "on" when pulled to ground.

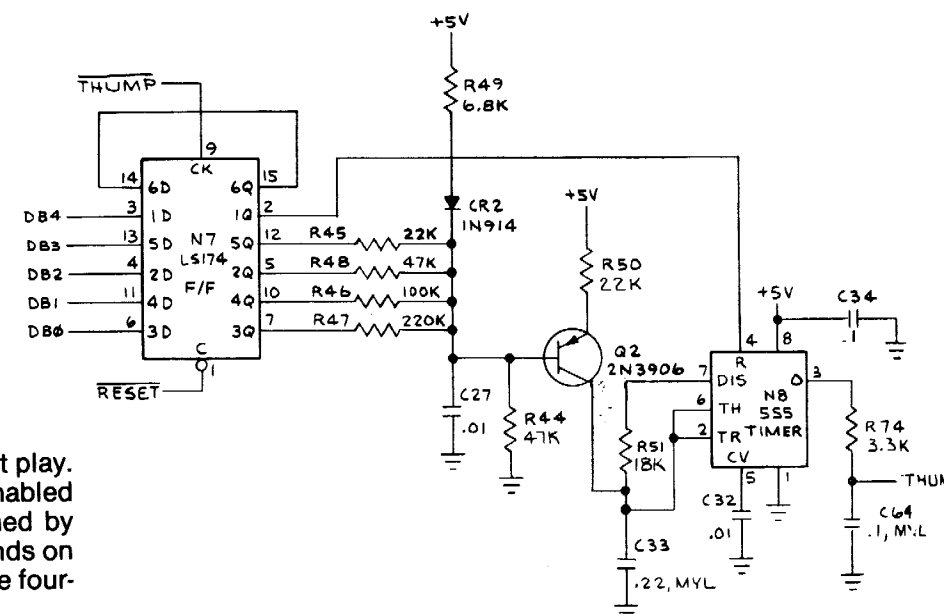
VIDEO INVERTER



The video inverter circuitry is only used in a cocktail game. In an upright game, pin 19 is unconnected and therefore floats. When pin 19 floats, transistor Q16 is turned off and transistor Q17 is turned on. Therefore, INV is -8.2 VDC and NONINV is about +8.2 VDC. The result is a non-inverted X-axis and Y-axis output.

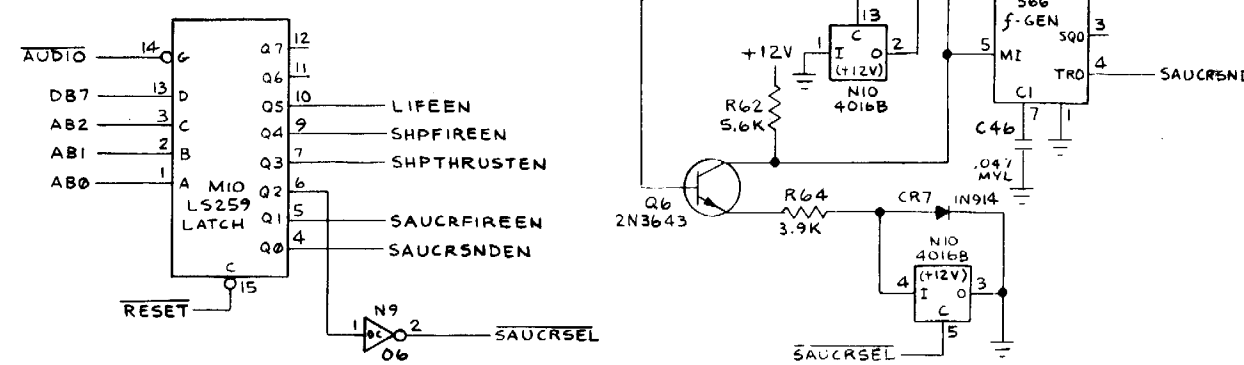
In a cocktail game, the wiring harness shorts connector J20's output pin 7 input pin 19. When the video of player 1 is being displayed, pins 7 and 19 are +5 VDC. This results in a non-inverted video output. When the video for player 2 is being displayed, pins 7 and 19 are grounded. This causes transistor Q16 to be turned on and Q17 to be turned off. Therefore, INV is +8.2 VDC and NONINV is -8.2 VDC. The result is an inverted X-axis and Y-axis output, causing the monitor's display to be up-side down.

OUTPUTS



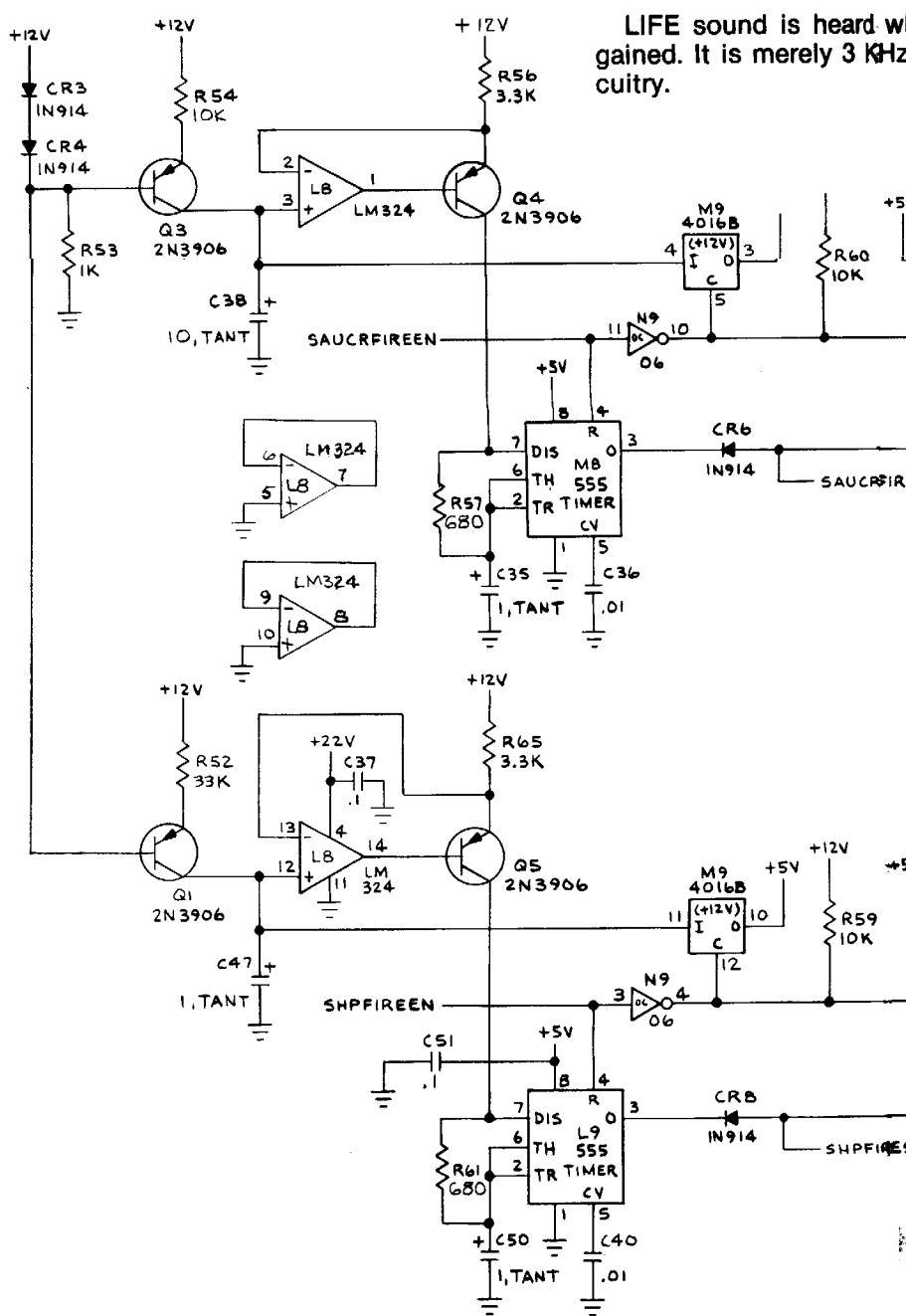
The THUMP sound is heard throughout play. The 555 is connected as an oscillator, enabled by N7 pin 2. The frequency is determined by the current coming out of Q2. This depends on its base voltage, which is derived from the four-bit code in N7.

The SAUCER sound is heard when an enemy saucer appears. The 566 is a voltage-controlled oscillator. Its modulating voltage is derived from the 555. The 555 is a low frequency oscillator. The effect is a warbling sound. SAUCRSEL changes some component values, in order to provide for 2 different saucer sounds.

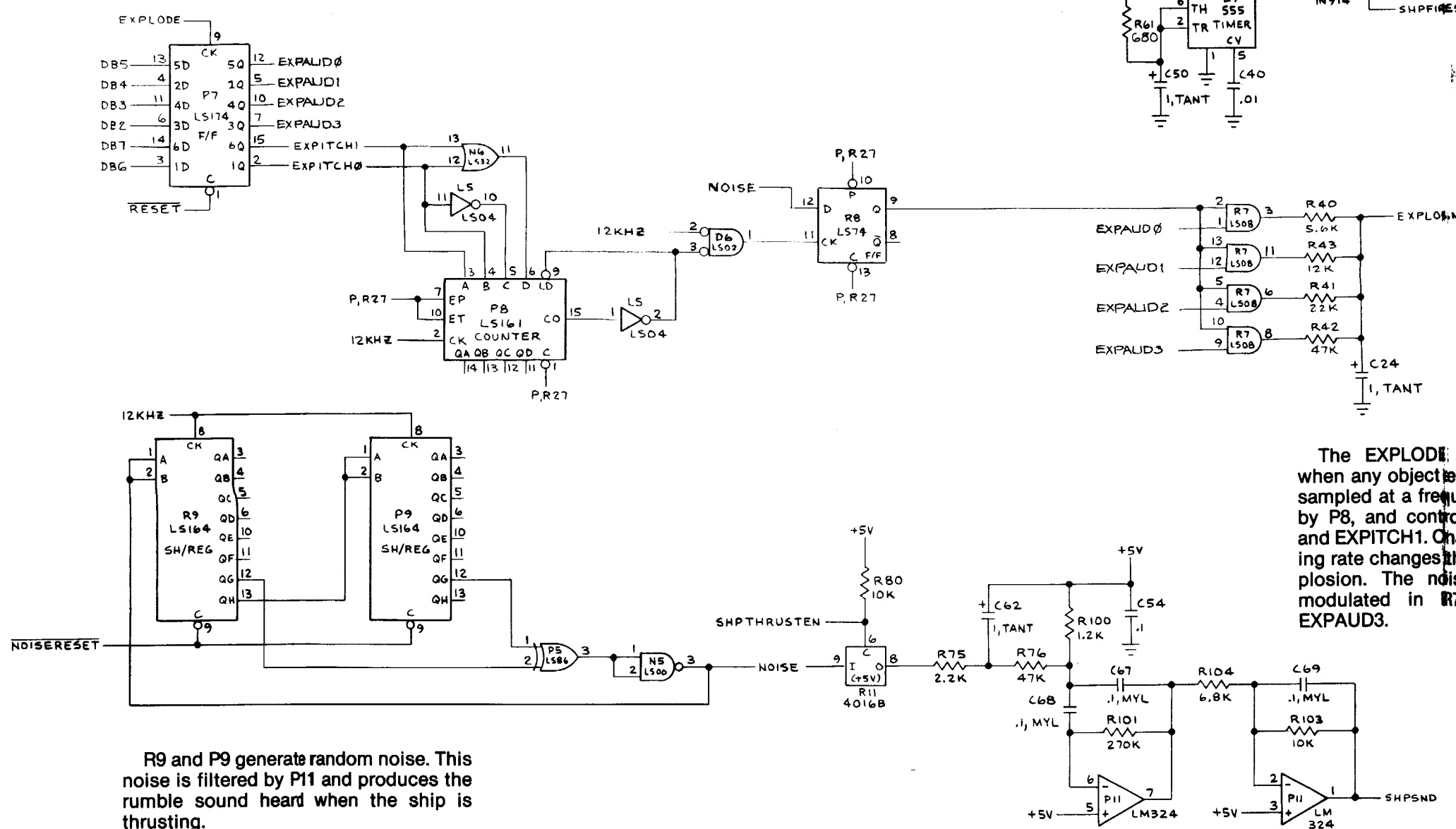


M10 latches control signals to enable different sounds.

The Fire sounds for the Saucer and the Space Ships are generated by two identical circuits. Each contain a 555 operating as a voltage-controlled oscillator. The Saucer Firesound is initiated by SAUCRFIREEN, and the Space Ship Fire sound is initiated by SHPFIREEN. Each of the 555s is configured in such a way that when they are enabled, they output a signal of a specific frequency and amplitude. This signal begins to decay immediately, both in frequency and amplitude, due to the discharge of the control capacitors (C38 & 39 for Saucer Fire Sound; C47 & 48 for Ship Fire Sound).



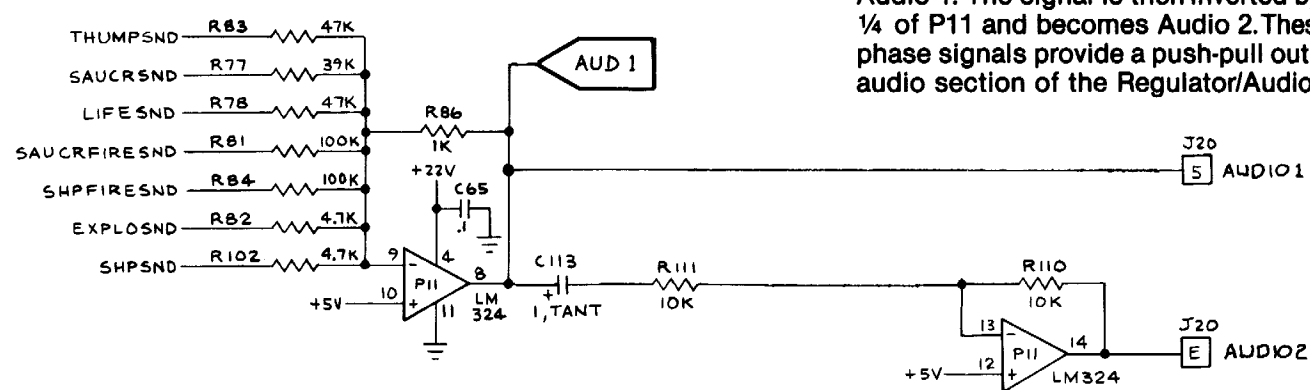
LIFE sound is heard when an enemy ship is gained. It is merely 3 KHz circuitry.



The EXPLODE sound is heard when any object is destroyed. The sound is sampled at a frequency of 3 KHz by P8, and controlled by EXPITCH1. The sound rate changes with explosion. The noise is modulated in P7 EXPALD3.

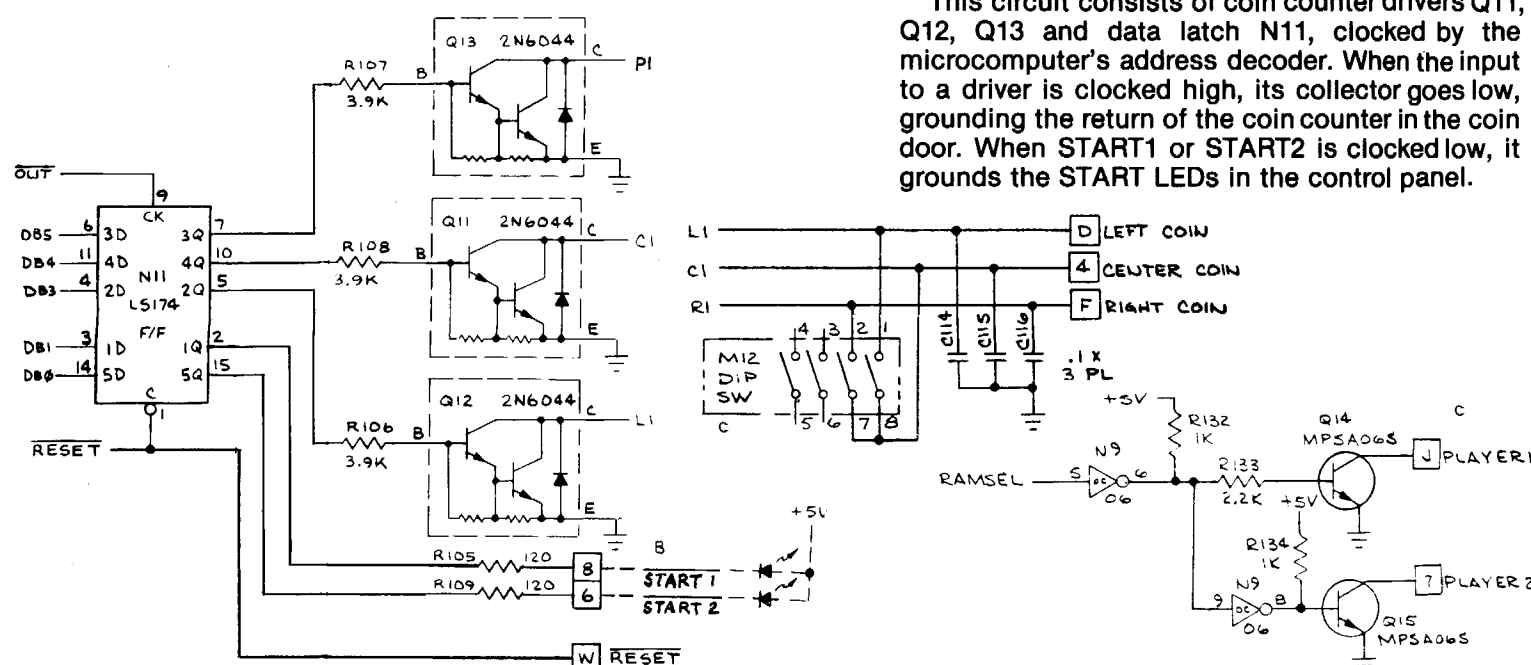
R9 and P9 generate random noise. This noise is filtered by P11 and produces the rumble sound heard when the ship is thrusting.

AUDIO OUTPUT



All sounds are mixed in 1/4 of P11. This is Audio 1. The signal is then inverted by another 1/4 of P11 and becomes Audio 2. These out-of-phase signals provide a push-pull output to the audio section of the Regulator/Audio PCB.

LAMP, LED, AND COIN COUNTER OUTPUT

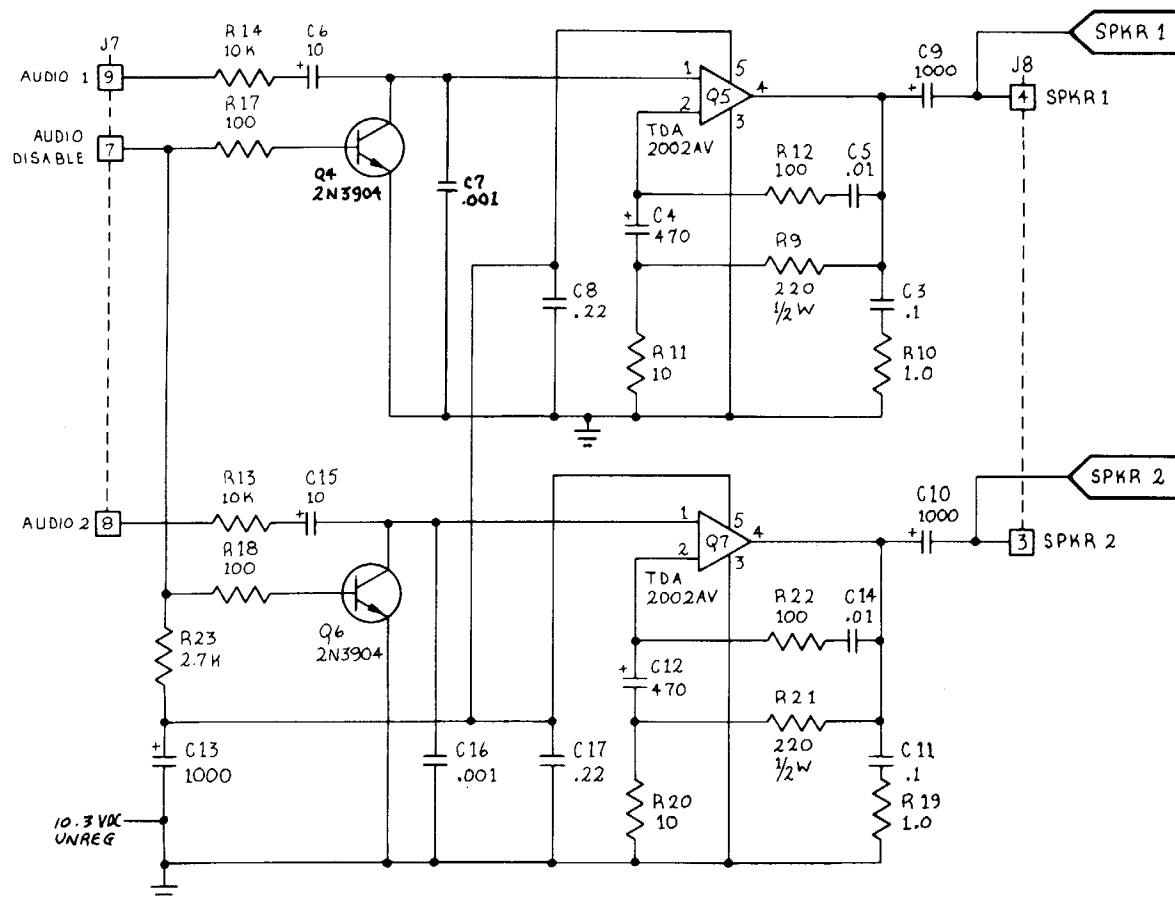


This circuit consists of coin counter drivers Q11, Q12, Q13 and data latch N11, clocked by the microcomputer's address decoder. When the input to a driver is clocked high, its collector goes low, grounding the return of the coin counter in the coin door. When START1 or START2 is clocked low, it grounds the START LEDs in the control panel.

PART OF REGULATOR/AUDIO PCB

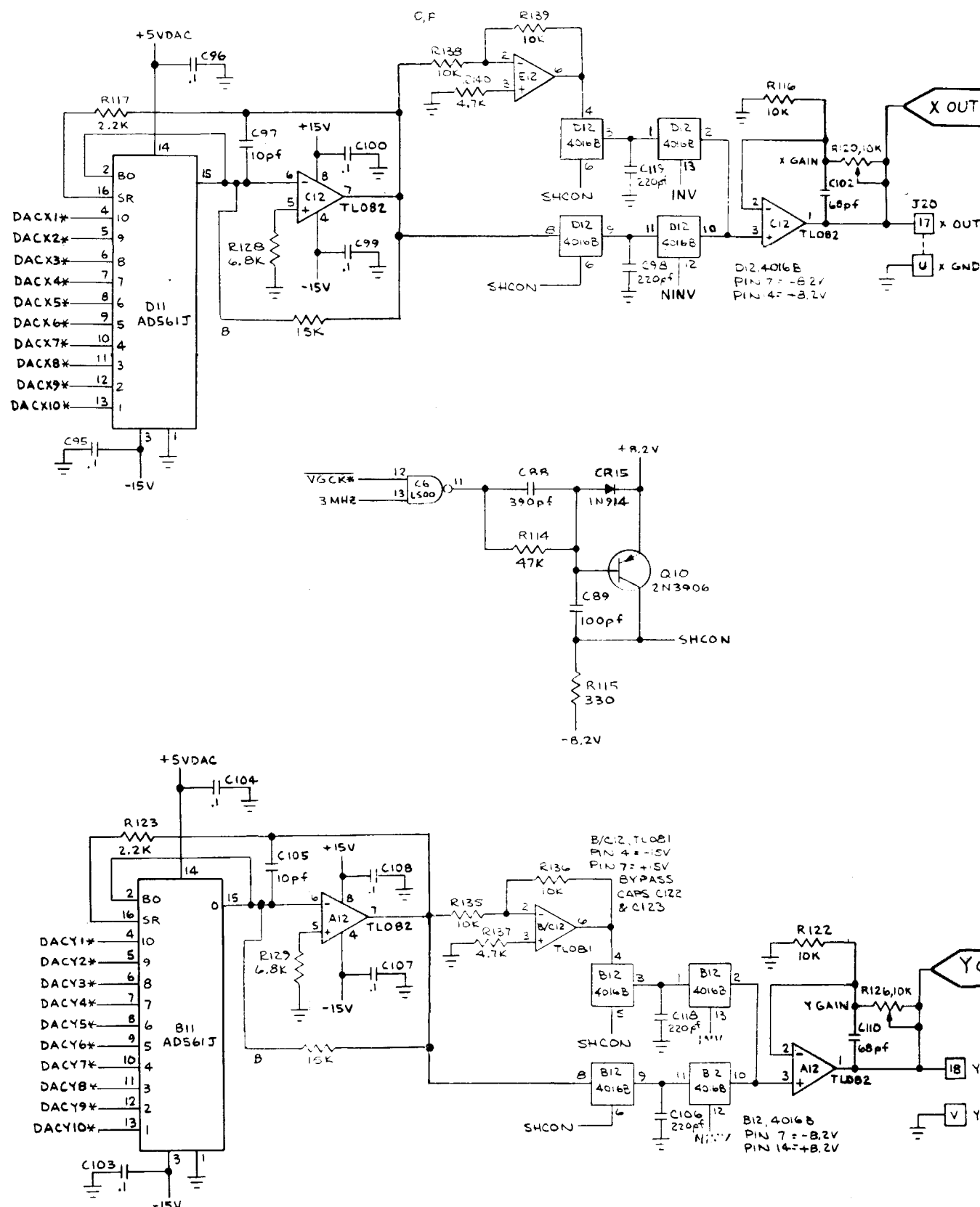
NOTE: AUDIO AMPLIFIER IS PART OF REGULATOR/AUDIO PCB AND IS REPEATED ON SHEET 1, SIDE A.

Audio inputs AUDIO 1 and AUDIO 2 receive out of phase signals for push-pull operation. AUDIO DISABLE is permanently grounded for continuous audio amplification.



denotes a test point

VIDEO OUTPUTS



The video output circuit consists of three individual circuits; X axis, Y axis, and Z axis video output circuits. The X axis and Y axis video output circuits each consist of a digital-to-analog converter (DAC), current-to-voltage converter, two sample and holds, and amplifier. The Z axis video output circuit consists of a shift register and a summer.

X and Y Outputs

The DACs (D11 and D12) each receive binary numbers from the vector generator's position counters outputs. These numbers represent the location of the beam on the monitor. For the non-inverted X axis, the numbers range from 0 to 1023, where 0 is at the far left of the monitor screen, 512 is at the center, and 1023 is at the far right. For the non-inverted Y axis, the numbers range from 128 to 996, where 128 is at the bottom of the monitor screen, 512 is at the center, and 996 is at the top. When the X axis and Y axis are inverted, the monitor picture is turned upside down. This is used for a two-player cocktail game.

The DACs convert these binary number inputs to current outputs. The DACs' current outputs are applied to the pin 6 inputs of current-to-voltage converters C12 and A12.

From the current-to-voltage converters, the signal is fed to two sample-and-hold circuits: One is non-inverted and the other is inverted. The non-inverted sample and hold consists of one stage of analog switch D12 and capacitor C98 for the X axis, and B12 and C106 for the Y axis. The inverting sample and hold consists of inverter E12, one stage of analog switch D12, and capacitor C119 for the X axis and B/C12, B12 and C118 for the Y axis.

The sample and hold circuits are controlled by SHCON (sample and hold control). SHCON is derived by gating 3 MHz from the microcomputer clock circuitry and VGCK* from the vector generator's state generator. The result of these inputs insures that the non-inverted and inverted analog signals that are applied to the analog switches have sufficiently stabilized before being applied to the sample and hold capacitors.

The output swing of SHCON is -8 to +8 VDC. When SHCON is high, the voltage charges or discharges the sample-and-hold capacitors to the X and Y analog voltage value. The voltages are then applied to the inputs of the second analog switch. These switches select either the non-inverted or inverted X-axis and Y-axis outputs. The outputs are then amplified by the second stages of C12 and A12 for an impedance-matched output to the X and Y inputs to the monitor. Since the monitor doesn't have field-adjustable X and Y gains, the gains are adjustable by variable resistors R120 and R126.

Z Output

The Z axis video output receives six inputs. BVLD (beam valid), from the output of the vector generator's position counters, tells the Z axis to draw the line. BLANK (vector line blank), from the vector generator's state machine, tells the Z axis to stop drawing a line. SCALE0 thru SCALE3 (grey level shading scale), from the output of the vector generator's data latch, tells the Z axis the grey level shading of the line that is being drawn on the monitor.

When BVLD and BLANK are both high, a high is clocked through shift register K9 that turns transistor Q3 off. This allows the scale inputs to be passed through transistor Q2. When BLANK goes low, a low is clocked through K9, transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

The scale inputs at the base of transistor Q1 determine Q1's emitter voltage, during the line draw period. The SCALE0 thru SCALE3 resistors R36 thru R39, resistor R35, and resistor R40 result in a range of about +1.0 VDC when all are low and +4.0 VDC when all are high. The emitter of Q1 follows at about +1.7 to 4.7 VDC, while the emitter of transistor Q2 follows at about +1.0 to 4.0 VDC. This output is applied to the Z input of the monitor. Since there are brightness and contrast controls in the monitor, there are no adjustments in this circuit.

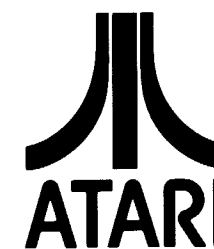
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ASTEROIDS

Switch Inputs, Coin Counter, LED and Audio Outputs

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